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The reduction of input open-fault in a CMOS Schmitt-Trigger inverter

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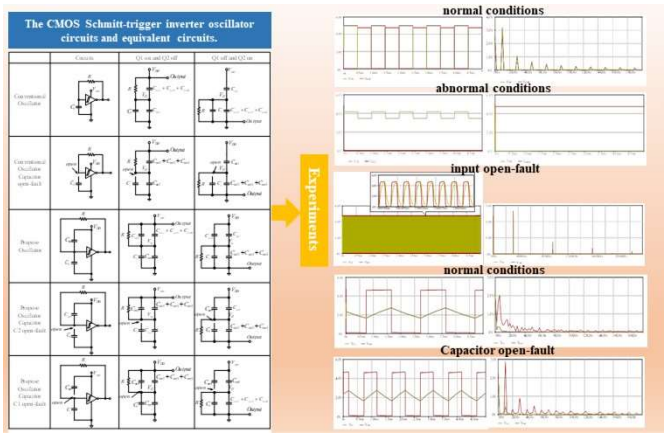
Abstract

The failure of the CMOS Schmitt-trigger inverter open-fault and capacitor open-fault in the case of a CMOS Schmitt-trigger inverter oscillator circuit cause a self-oscillation of the device. It leads to the high frequency to be emitted on the output side, because the balance of internal smaller parasitic capacitance approximately 5 – 20 pF. In this article, the reduction of CMOS Schmitt-trigger inverter open-fault and capacitor open-fault in the case of a CMOS Schmitt-trigger inverter oscillator circuit is presented, by adding a capacitor between the Gate pin and Drain pin of Q_1 by demonstration illusion of an equivalent circuit. This causes the internal parasitic capacitance to unbalance, then the self-oscillation in the case of input open-fault will not accord. Besides in the case of an oscillator circuit, the feedback resistor is not combined with the internal parasitic capacitance. However, it is combined it is with the added capacitance, the higher frequency self-oscillation does not occur. The circuit was tested with a PSPICE computer simulation program.



Keywords: Fail-safe; Open-fault; Self-oscillation; CMOS inverter

1. Introduction

There are many potential causes of failure in a CMOS Schmitt-trigger inverter, such as the input pin is open or broken. It causes self-oscillation due to the parasitic capacitance within approximately 5 – 20 pF presented at the semiconductor junction on both the PMOS and NMOS sides. The latent capacitor caused self-oscillation [1] because the voltage supply is approximately 5 V when splits in half. The value is 2.50 V, which is equal to the threshold voltage of the ICs. This fluctuation produces a pulse signal with a duty cycle of 50%. Correcting this fluctuation is achieved by unequalizing the parasitic capacitance within the CMOS IC by connecting a capacitor that is significantly larger than the internal parasitic capacitance at the VG point relative to the ground. Alternatively, a small metal plate connected to the ground pin of the IC can be used to distribute the signal [2, 3].

Moreover, the critical failure of the CMOS Schmitt-trigger inverter oscillator circuits is an open failure of the capacitor input. This causes

the self-oscillation of the CMOS Schmitt-trigger inverter produces a higher frequency pulse signal at the output due to the combination of the feedback resistance [4] with the internal parasitic capacitance of the smaller semiconductor at approximately 5 – 20 pF. Solve the CMOS Schmitt-trigger inverter self-oscillation problem in circuits by [2 – 4] adding capacitors to capacitance to the parasitic capacitance within the inverter. With this makes the combined internal and external capacitance differ between on and off operation. In this case, it can be used as a 4-pin special capacitor connected as the input capacitor. When an open failure occurs, the capacitors are cut off and separated into two halves.

Both failure cases, the solution to avoid the failures is to increase the capacitor between V_G and V_{DD} supply, which increases the capacitance of the internal capacitor. The PMOS side is greater than the NMOS side so it does not cause self-oscillation in the case of a buffer circuit. Further, it does not cause high-frequency oscillation in the case of oscillator circuits because the capacitance is combined with the delay capacitor. The results were confirmed by using PSPICE computer simulation program.

2. Materials and Methods

The CMOS inverter equivalent circuit consists of PMOS (Q_1), NMOS (Q_2), and parasitic capacitance [5 – 6]. Under normal situations, when the input is low, PMOS Q_2 is closed and NMOS Q_1 is open. Conversely, when the input is high, the position is with Q_1 off and Q_2 on when the input is at the MOSFET voltage level. One of them turns the other on and off. The CMOS inverter structure, as illustrated, is shown in Fig. 1.

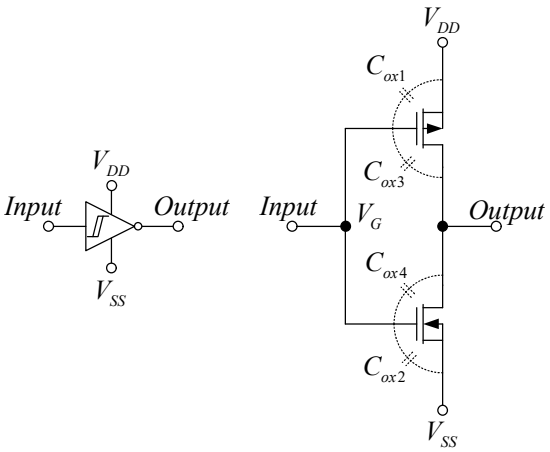


Fig. 1 CMOS inverter and schematic circuit with junction parasite capacitance.

Situation inputs open-fault Q_1 and Q_2 are opened and closed by the interference caused by variations within the system or the external impact of the environment. When a power source is supplied on the assumption that both Q_1 and Q_2 are turned off, V_G is obtained from Eq. (1).

$$V_G = \frac{C_{ox2}}{C_{ox1} + C_{ox2}} V_{DD} = \frac{1}{2} V_{DD} \qquad (1)$$

Since C_{ox1} and C_{ox2} are connected in series with V_{DD} voltage, if the capacitance of C_{ox1} and C_{ox2} are similar, V_{DD} is $V_{DD}/2$, When Q_2 is turned off, the V_G voltage will increase due to the C_{ox2} charge. This corresponds to the fact that the input to the CMOS inverter is high.

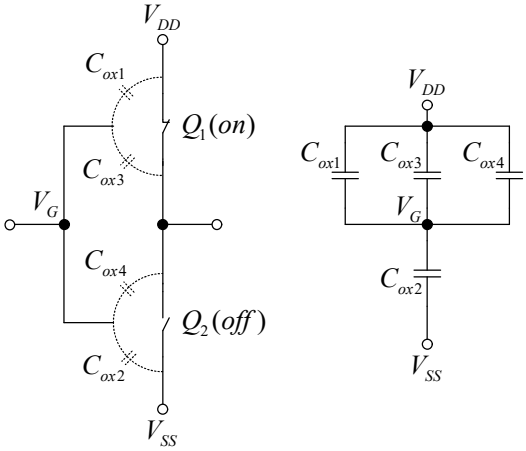


Fig. 2 Equivalent circuit of Q_1 active (on) and Q_2 not active (off).

The equivalent circuit in Fig. 2, the combination and connection of capacitances change when Q_2 is turned off and Q_1 remains on, V_G can be given by Eq. (2).

$$V_G = \frac{\frac{1}{C_{ox2}}}{\frac{1}{C_{ox1}+C_{ox3}+C_{ox4}}+\frac{1}{C_{ox2}}} V_{DD} \quad (2)$$

When V_G is risen, Q_1 is not activated (off) and Q_2 is activated (on), as shown in the equivalent circuit in Fig. 3.

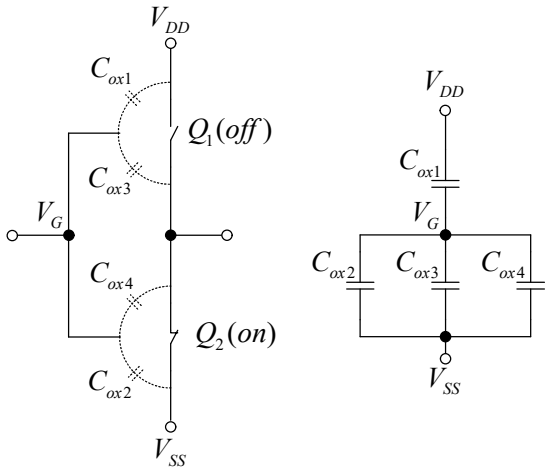


Fig. 3 Equivalent circuit of Q_1 not active (off) and Q_2 active (on).

The combination and connections of capacitance are changed, the V_G changes are defined by Eq. (3). The V_G voltage drop is due to the charge of C_{ox2}, C_{ox3}, and C_{ox4}, which led to a low value of CMOS inverter.

$$V_G = \frac{\frac{1}{C_{ox2}+C_{ox3}+C_{ox4}}}{\frac{1}{C_{ox2}+C_{ox3}+C_{ox4}}+\frac{1}{C_{ox1}}} V_{DD} \quad (3)$$

Equations (2) and (3), as mentioned above, repeat themselves and cause their oscillations of CMOS inverters, CMOS inverters structure are common, which the same as CMOS logic gates. The application of inverters and CMOS logic gates, causing their oscillation by an input open-fault.

The idea solution is adding the capacitor between the V_G and the V_{DD} supply, which increases the capacitance of the internal capacitor. The PMOS side is greater than the NMOS side, so it does not cause self-oscillation in the case of a buffer circuit because the voltage at the V_G point is not equal to $V_{DD}/2$ (C_{ox5}>>C_{ox1}). The circuit and equivalent circuit are shown in Fig. 4.

The combination and connection of capacitance is changed as well as the V_G as defined by Eq. (4).

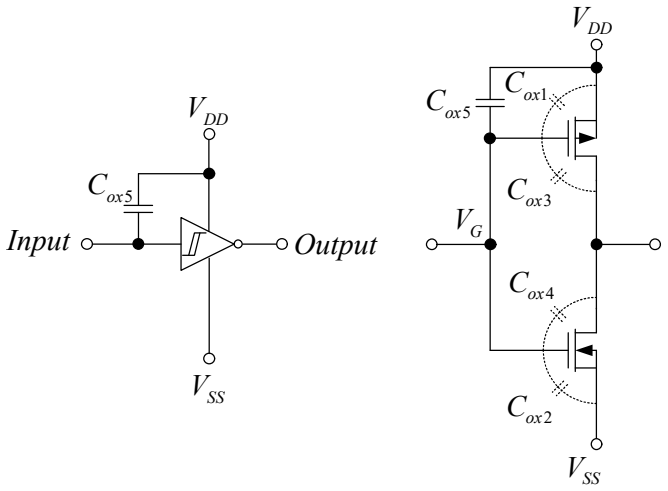


Fig. 4 The proposed equivalent circuit.

$$V_G = \frac{C_{ox2}}{C_{ox1}+C_{ox2}+C_{ox5}} V_{DD} \quad (4)$$

When Q_1 is activated (on) and Q_2 is not activated (off), the external capacitance C_{ox5} is connected to V_{DD} and V_G point, as shown in Fig. 5. The voltage at the V_G point is obtained from the sum of the capacitance values, as shown in Eq. (5).

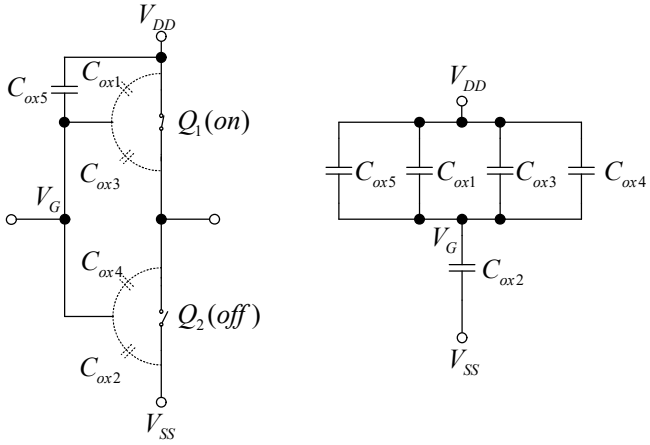


Fig. 5 The proposed equivalent circuit of Q_1 active (on) and Q_2 not active (off).

$$V_G = \frac{\frac{1}{C_{ox2}}}{\frac{1}{C_{ox5}+C_{ox1}+C_{ox3}+C_{ox4}}+\frac{1}{C_{ox2}}} V_{DD} \quad (5)$$

When Q_1 is not activated (off) and Q_2 is activated (on), the external capacitor is still at the V_G point and V_{DD}, as shown in Fig. 6, while the voltage is obtained at the V_G point, as shown in Eq. (6).

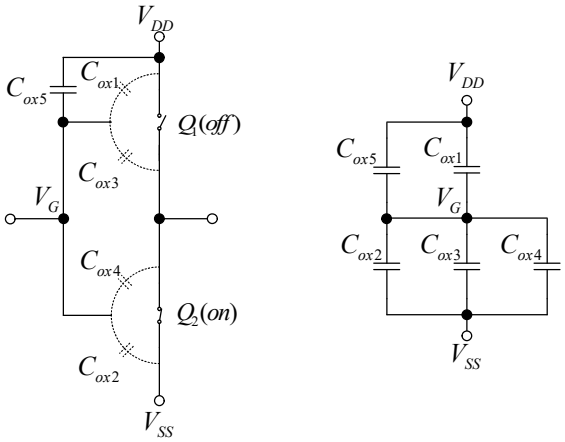


Fig. 6 The proposed equivalent circuit of Q_1 not active (off) and Q_2 active (on).

$$V_G = \frac{\frac{1}{C_{ox2}+C_{ox3}+C_{ox4}}}{\frac{1}{C_{ox2}+C_{ox3}+C_{ox4}}+\frac{1}{C_{ox1}+C_{ox5}}} V_{DD} \quad (6)$$

In case, when the CMOS Schmitt-trigger inverter as a relaxation oscillator circuit, a capacitor and a resistor are commonly used in the circuit to delay the oscillation. The proposed method used one additional capacitor, allowing the signal generator to be equal to the two capacitors combined, which can be calculated as in Eq. (7) and (8).

$$f = \frac{1}{2R(C_1+C_2)\ln\left(\frac{V_{T+}}{V_{T-}}\right)} \quad (7)$$

$$f \approx \frac{1}{0.8R(C_1+C_2)} \quad (8)$$

Fig. 7 shows a comparison of the results of failure in the event of an open capacitor in a relaxation oscillator circuit between a conventional oscillator circuit and the proposed circuit. It can be seen that, in a conventional circuit, the operation of the oscillator circuit can be continued to generate a signal. When there is a failure of the open capacitor because the feedback resistors are still connected at the V_G point. Further, combining the small value internal parasite capacitance of the ICs can produce a high-frequency signal. In the proposed circuit, there are two externally connected capacitors, C_1 and C_{ox5}, that are connected in series, giving capacitance equal to $C_1 + C_{ox5}$. If one out of two capacitors open-fault, there will still be another capacitor connected, resulting in a doubling of the frequency value, but no high-frequency signal.

3. Results and Discussion

The circuit performance results were simulated using a Pspice to test the CMOS Schmitt-trigger inverter open failure effect in the case of a buffer circuit and relaxation oscillator circuit. The CMOS Schmitt-trigger inverter input open-faults, tested with a pulse signal of 1 kHz at the input and the output shows an out of phase signal, as shown in Fig. 8. If there is an open failure, the input self-oscillates at the same frequency as the source without affecting the output as the input voltage range between $3.50 - 4.20$ volts that no output voltage signal, as shown in Fig. 9(a). In a real circuit, an output signal may occur if another failure occurs. The circuit presented an external capacitor on the input pin with a positive voltage source does not oscillate on its own. There is no input voltage signal, resulting in constant logic 1 output, as shown in Fig. 9(b). The oscillator circuit 1 kHz, when there is an open failure of a capacitor, the capacitance of the circuit decreases, a high-frequency inversion of approximately 30 MHz occurs, as shown in Fig 10.

The additional capacitor is connected to the oscillator circuit, as shown in Fig. 7, two external capacitors are formed. The total capacitance is obtained from the sum of the two capacitance values. When a failure occurs in one of the capacitors, no high-frequency oscillation occurs, as shown in Fig. 11 and 12.

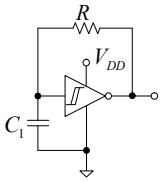
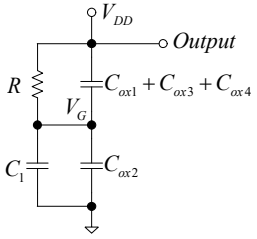
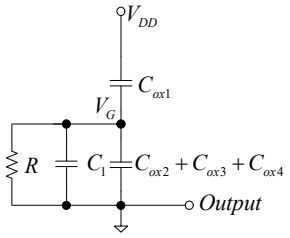
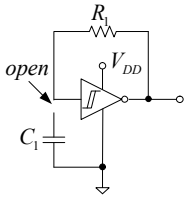
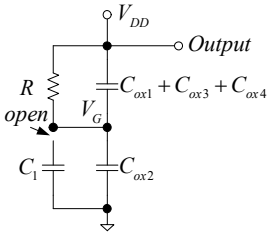
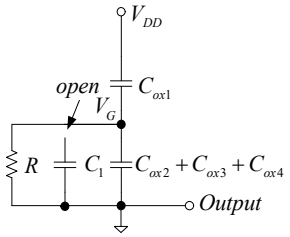
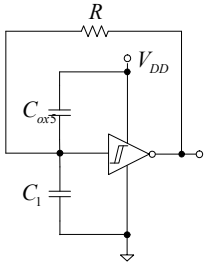
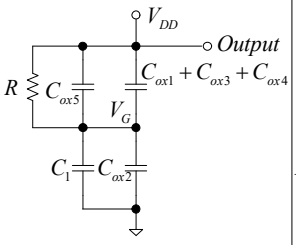
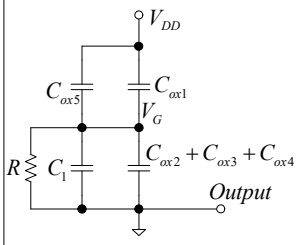
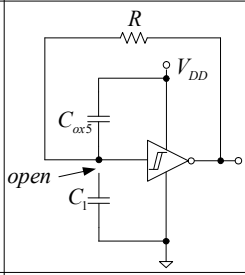
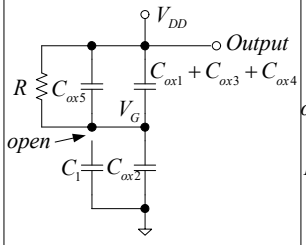
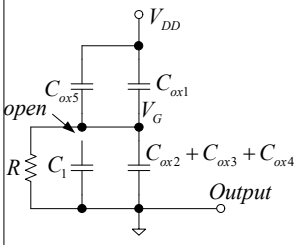
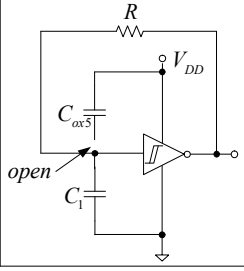
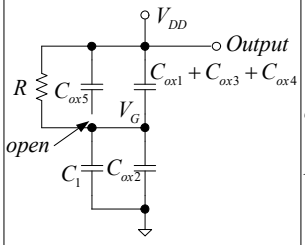
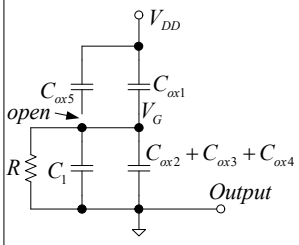
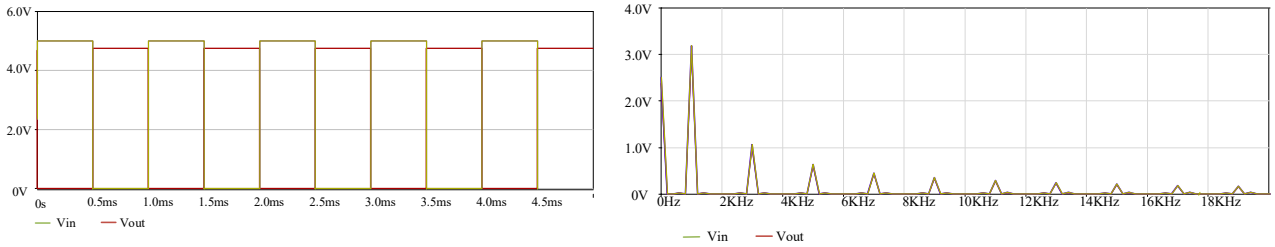
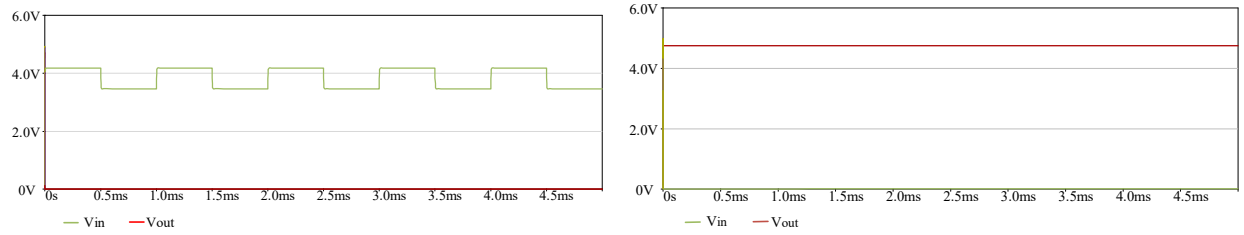
	Circuits	Q_1 on and Q_2 off	Q_1 off and Q_2 on
Conventional Oscillator			
Conventional Oscillator Capacitor open-fault			
Propose Oscillator			
Propose Oscillator Capacitor C2 open-fault			
Propose Oscillator Capacitor C1 open-fault			

Fig. 7 The CMOS Schmitt-trigger inverter oscillator circuits and equivalent circuits.



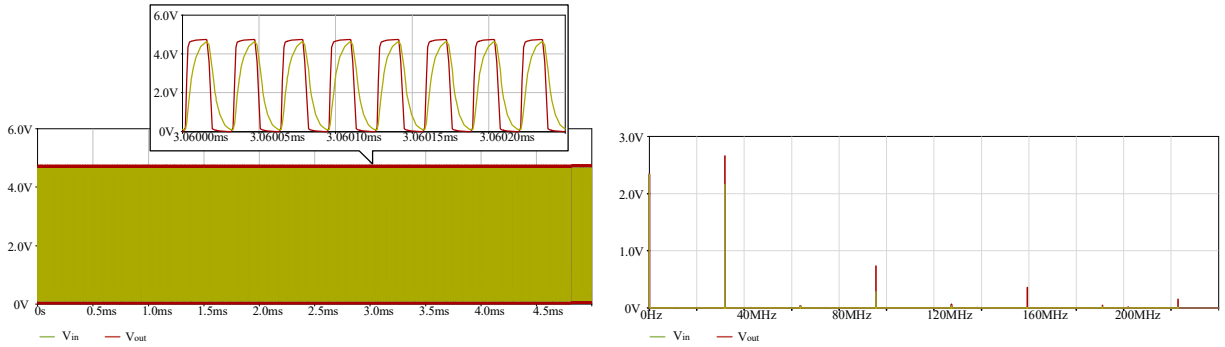
a) Voltage waveform b) FFT

Fig. 8 The CMOS Schmitt-trigger inverter buffer circuit normal conditions.



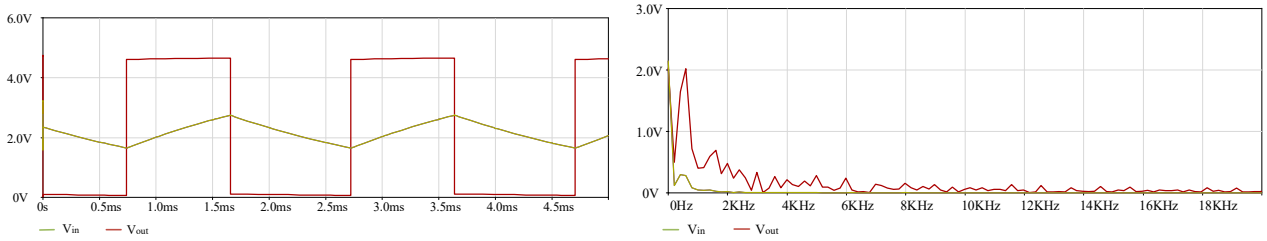
a) The input self-oscillates b) The output constant logic 1

Fig. 9 The CMOS Schmitt-trigger inverter buffer circuit abnormal conditions.



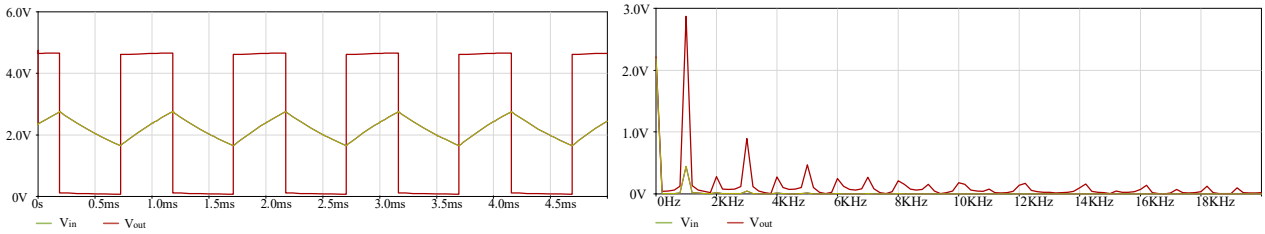
a) Voltage waveform b) FFT

Fig. 10 The CMOS Schmitt-trigger inverter oscillator circuit input open-fault.



a) Voltage waveform b) FFT

Fig. 11 The proposed CMOS Schmitt-trigger inverter oscillator normal conditions.



a) Voltage waveform b) FFT

Fig. 12 The proposed CMOS Schmitt-trigger inverter oscillator circuit capacitor open-fault.

4. Conclusion

The reduction of the CMOS Schmitt-trigger inverter open-fault and capacitor open-fault in the case of a CMOS Schmitt-trigger inverter oscillator circuit is achieved by adding a capacitor between the Gate pin and Drain pin of Q_1 by an illusion of equivalent circuit. This causes the internal parasitic capacitance to unbalance so that it does not cause self-oscillation in the case of input open-faults. The result is a fixed input signal of logic 0 and a fixed output signal of logic 1. In the case of the oscillator circuit, the feedback resistor is not combined with the internal parasitic capacitance but is combined with the add capacitance so that the higher frequency self-oscillation does not occur. The solution is to divide the capacitance in half, so the frequency is doubled.

5. Acknowledgement

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6. References

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