การพัฒนาวงจรอินเวอร์เตอร์แรงดันเอาต์พุต 5 ระดับ
The Implementation of a Single Phase Five-Level Inverter

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บทคัดย่อ

บทความวิจัยนี้มีวัตถุประสงค์เพื่อนำเสนอการพัฒนาวงจรทบระดับแรงดันไฟฟ้ากระแสตรงโดยใช้สวิตช์ 2 ตัว ที่ได้รับการนำเสนอมาแล้วก่อนหน้านี้ โครงสร้างของวงจรประกอบด้วยตัวเหนี่ยวนำ 1 ตัว สวิตช์ขับ 2 ตัว ไดโอด 9 ตัวและตัวเก็บประจุ 3 ตัว ออกแบบให้เป็นวงจรทบระดับแรงดัน 4 ระดับที่สามารถปรับค่าแรงดันด้านเอาต์พุตได้เท่ากันทุกระดับชั้น ในส่วนระบบของวงจรอินเวอร์เตอร์นั้น จะเป็นการนำวงจรทบระดับแรงดันไฟฟ้ากระแสตรงมาเชื่อมต่อกับชุดวงจรไดโอดแคลมป์อินเวอร์เตอร์ 5 ระดับ โดยมีการควบคุมรูปแบบการสวิตช์ตามที่กำหนด ดังนั้นสัญญาณแรงดันที่ได้จากวงจรทบระดับแรงดันในภาคแรกจะกลายเป็นแรงดันอินพุตให้แก่วงจรอินเวอร์เตอร์ในภาคหลัง ซึ่งแรงดันเอาต์พุตที่ได้จะมีลักษณะเป็นขั้นบันได การทำงานของทั้งสองภาคจะทำงานในความถี่สูง ยืนยันการทำงานของวงจรที่นำเสนอด้วยการจำลองการทำงานด้วยโปรแกรม PSIM

คำสำคัญ : วงจรทบระดับแรงดันไฟฟ้ากระแสตรง 2 สวิตช์; คอนเวอร์เตอร์หลายระดับ; วงจรทบระดับแรงดัน; ไดโอดแคลมป์อินเวอร์เตอร์ 5 ระดับ

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Abstract

The objective of this research paper is to discuss the development of a two-Switch based DC-DC multilevel Boost Converter (2SBC) recently proposed. The purposed DC-DC converter circuit consists of an inductor, 2 driven switch, 9 diodes and 7 capacitors. This circuit has 4-levels boost converter which is able to regulate output voltage in all level. For the implementation of an inverter system, boost convert interfaced a five-level diode clamped inverter configuration is developed under switching control schemes. The 2SBC of the first stage become the input voltage of the inverter, resulting in a staircase waveform for the inverter output voltage. Both stages are operated at a high switching frequency. PSIM Simulated is presented to validate the proposed inverter.

Keywords : 2SBC; multilevel converter; boost converter; five-level diode clamped inverter

Introduction

In most renewable energy system like solar cell and fuel cell, the voltage obtained is low and has to be boosted up for meaningful utilization. A boost converter was used to obtain the required high voltage gain (Rosas-Caro, J.C. et al., 2011; Rosas-Caro, J.C. et al., 2008; Tomaszuk, A. and Krupa, A., 2011). Though cascading of boost converters and multilevel converter achieved the DC/AC inverter. It resulted in the better output signal voltage and current those are pretty close to a sine wave.

Multilevel converters have been attracting an increasing amount of consideration in high voltage converter with low voltage devices and high power qualities. Various topologies for multilevel inverters have been introduced and widely studied (Rodriguez, J. et al., 2002; Chenchen, W. and Yondong, L., 2009). The most considerable of these topologies are Neutral Point Camped (NPC) also called diode clamped, Flying Capacitor (FC) and Cascaded Multilevel (CM). Multilevel converters synthesis stair case output voltage which is closer to sinusoidal waveform. By increasing the number of output level, the harmonic content of voltage and current waveform are reduced.

The diode clamped converter is widely used in transformerless grid connected system because of its minimum number of active power components and shared DC link voltage (Muhammad H.R., 2011). Due to the structure of the diode-clamped converter, it suffers from neutral point voltage balancing. There are two types of voltage balancing problems, the midpoint unbalance and the central capacitor discharge

several researches have been proposed for solving both problems (Adam, G.P., et al., 2008; Rosas-Caro, J.C., et al., 2008; Stala, R., 2011). The two-Switch based DC-DC multilevel Boost Converter (2SBC) is a topology recently proposed (Leardpan, P. and Singthong, P., 2013), which can be used to overcome those challenges.

This paper proposes the development of the 2SBC to boost the DC voltage from an energy source to be connected with a five-level diode clamped converter, resulting in a staircase waveform for the inverter output voltage. A Fourier analysis of the output waveform is performed.

Methodology

Four-level converter

The two-level DC to DC boost converter with improved voltage gain has been introduced by (Leardpan, P. and Singthong, P., 2013). Figure 1 shows a schematic, it is based on 2 switches, 1 inductor, 5 diodes and 4 capacitors.

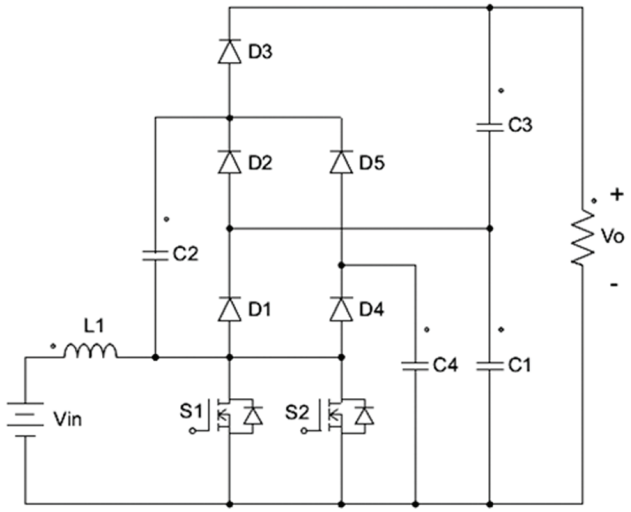


Figure 1 The 2SBC schematics

The main driven switch S1 and the auxiliary driven switch S2 is operated at each switching frequency, the main S1 is driven at frequency of F hertz while the auxiliary switch S2 is driven at F/2 hertz. The average output power of the load-resister can be controlled by only adjusting the duty cycle of the main switch S1. The output voltage across the load can be expressed as;

$$Vo = \frac{4 \times Vin}{1 - D} \quad (1)$$

The principle of this converter will be explained, assume that the switches (S1 and S2) is switching with duty cycle of 0.5.

During some switches are on state, the inductor is connect to Vin voltage. Current flows through an inductor L1, switch S1 and/or S2. Both capacitors C1 and C4 charge C2 through the D2. When all switches turn off, the energy in the inductor is transferred to the capacitors C1 and C4 through D1 and D4 respectively. C3 is charged by C2.

In this paper, the proposed converter circuit is shown in Figure 2. By rearranging the 2SBC structure and setting the output level to four. The output voltage across the load can be expressed as;

$$Vo = \frac{8 \times V_{in}}{1 - D} \quad (2)$$

The proposed converter, it is a central source variation. As a natural extension of the voltage multiplier in the negative part, reducing the current stress in the lower devices (Rosas-Caro, J.C. et al., 2008).

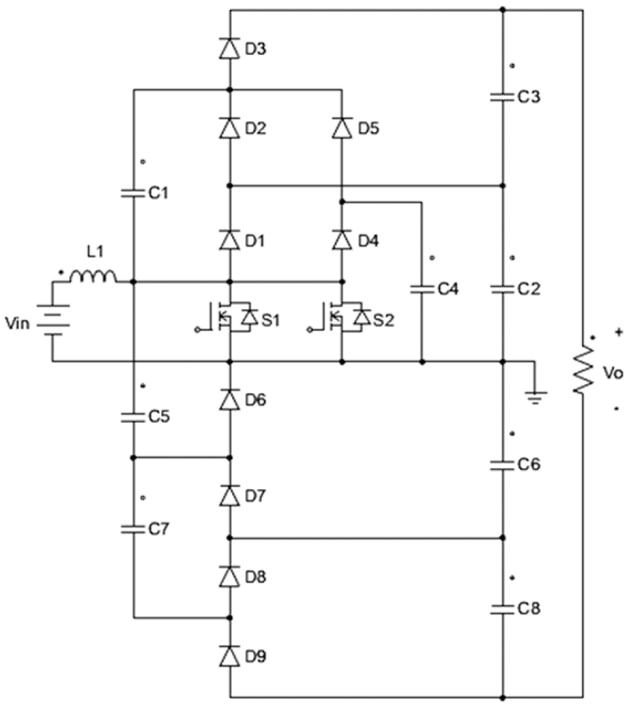


Figure 2 The proposed four-level converter

Five-level diode clamped converter

Diode clamped converter also called the Neutral-Point Clamped (NPC) converter. The circuit topology was first presented in 1980 (Nabae, A. et al., 1981) as a three-level converter.

In this paper, the five-level diode clamped converter was chosen. The proposed converter is shown in Figure 3.

A five-level diode clamped converter, in which the dc bus consists of four capacitors, C1, C2, C3, and C4. For dc bus voltage Vdc, the voltage across each capacitor is Vdc/4 and also each device voltage stress is limited to Vdc/4 through clamping diode.

Table 1 shows the voltage level and their corresponding switch state. State condition "1" means the switch is on, and states "0" defines the switch is off.

Table 1 Five-level converter switching

V_L	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/4$	0	0	0	1	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

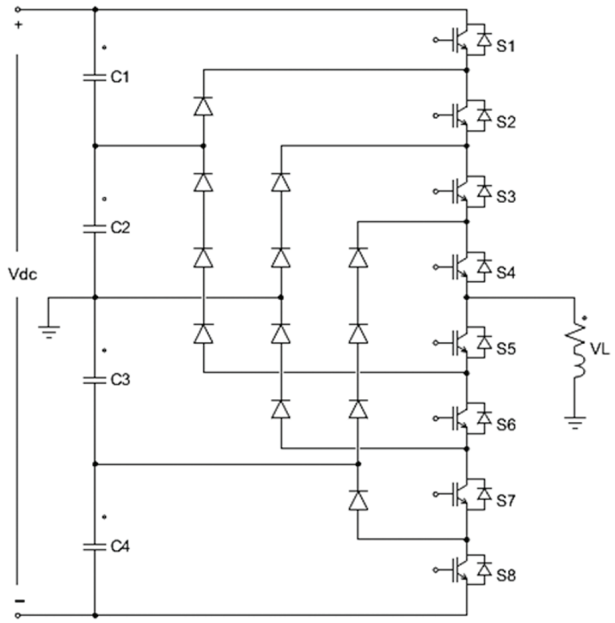


Figure 3 Five-level diode clamped converter

Five-Level inverter

The proposed inverter system is shown in Figure 4. The input stage is a four-level converter and the second stage is a five-level diode clamped converter, are connected in cascade. It is important that in the first stage, the left side capacitors are designed to transfer power from the lower level to the higher level so that their size are smaller than the right side capacitors which are the converters DC-link capacitors.

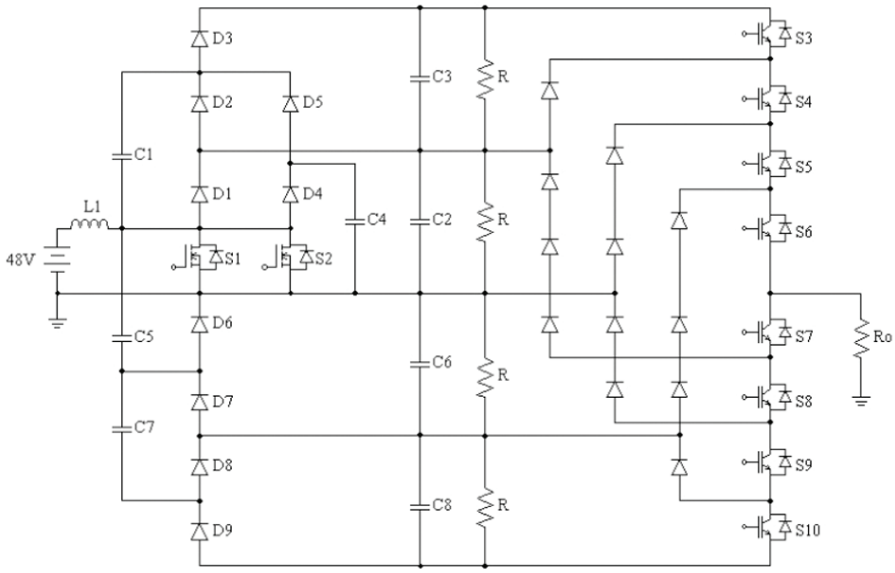


Figure 4 Proposed inverter with five-level output voltage

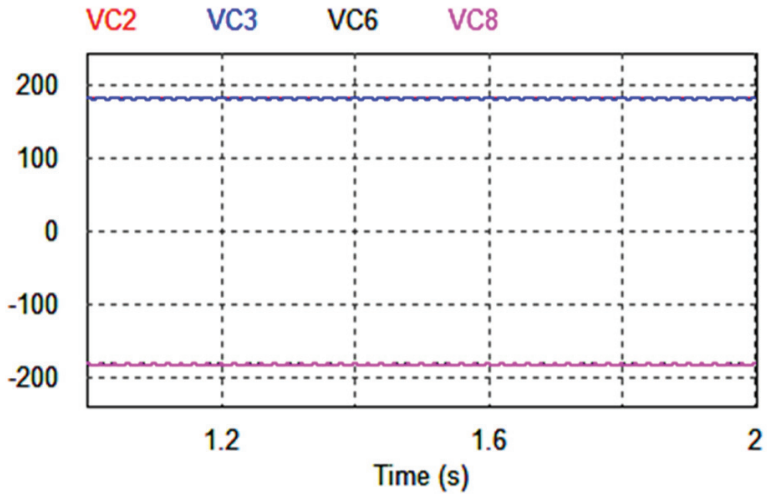
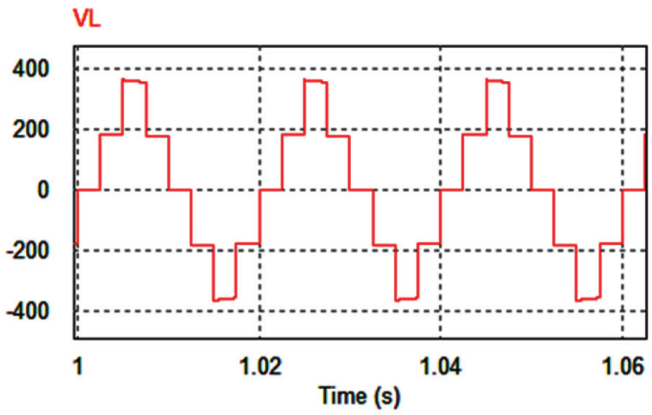


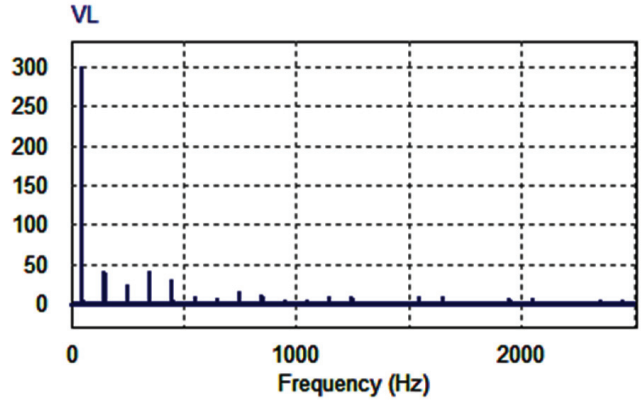
Figure 5 Voltage drop across each of capacitor

Table 2 Simulation parameters

Parameter	Value
Input voltage	48 V
Inductor L_1	1.5 mH
C_1, C_4, C_5, and C_7	220 μF
C_2, C_3, C_6, and C_8	500 μF
Switching frequency S_1	50 kHz
Switching frequency S_2	25 kHz
Duty cycle of S_1	0.47
Duty cycle of S_2	0.50
Load resistance	250 Ω



(a)



(b)

Figure 6 Simulation result waveform of the output voltage (a) and its frequency spectrum (b)

Simulation and Result

A simulation model of the proposed inverter is developed in PSIM environment. The parameters used for simulation work are given in Table 2.

The voltage drop across each of the output capacitors is shown in Figure 5. The average voltage drop of 181 volts across C2 and C3 is a positive value while the average voltage drop of 181 volts across C6 and C8 is a negative value. This validates the multilevel operation of the converter.

The staircase output voltage drop across the load and its frequency spectrum are shown in Figure 6 (a) and (b) respectively. The oscillogram of the output voltage of the five-level inverter is 220 Vrms and its THD is 17%.

Conclusion

In this paper, a single phase five-level voltage has been proposed. The structure circuit consists of 2 main parts, a four-level DC-DC boost converter and a five-level diode clamped converter, are connected in cascade. The first part is modified from a two-level DC/DC boost converter which up to 4 level. Also by rearranging the DC source to the central of the circuit structure, the set of symmetrical boosted voltage can be obtained. The function of this first part is to step up the voltage from 48V to around 720V with symmetrical voltage. Another part is a five-level diode clamped converter. It is used to generate a 220Vrms from a DC voltage. The output waveforms obtained from the PSIM simulation confirm the performance of the proposed converter.

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