New Cascaded Multilevel Inverter by Using Capacitor Based Basic Units with the Capability of Charge Balance Control Method

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ABSTRACT

In this paper, two new cascaded multilevel inverters based on new capacitor basic unit are proposed. In the proposed topologies, the same numbers of dc voltage source and capacitor are used that lead to decrease the number of required insulated dc voltage sources. In order to generate all positive and negative voltage levels (even and odd) at the output three different algorithms to determine the magnitude of voltage sources are proposed. Minimum number of used power electronic devices and lower amount of blocked voltage that is made by power switches are two main advantages of the proposed topologies. These features lead to decrease the installation space and total cost of the inverter. These are obtained by comparing the proposed topologies with several capacitor based cascaded multilevel inverters. In addition, in order to balance the used capacitors' voltage, a new charge balance control method is proposed. Finally, the correct performance of the proposed cascaded inverter is reconfirmed through experimental and simulation results on a five-level proposed inverter in EMTDC/PSCAD software program.

Keywords: Multilevel Inverters, Cascaded Multilevel Inverter, Capacitor Basic Unit, Power Electronic Devices, Charge Balance Control Method

1. INTRODUCTION

Multilevel inverters have received more attentions in comparison with conventional two level inverters. This is due to their advantages such as high power quality, better electromagnetic interference, lower harmonic components and lower value of dv/dt. In addition, it is possible to use of these inverters in high power and high voltage applications [1-2]. The multilevel inverters are classified into three main groups: diode clamped multilevel inverter, flying capacitor multilevel inverter and cascaded multilevel inverter [3-4]. There are not needed any diodes and flying capacitors in the cascaded multilevel inverter. In addition, this inverter consists of series-connected of several same basic units that lead to high modularity, high reliability and simplicity of control. These advantages lead to high attention to the cascaded multilevel inverter [5-7]. In this paper, the concentration is on the cascaded multilevel inverter. The cascaded multilevel inverter is classified into symmetric multilevel inverter with the same value of dc voltage sources and asymmetric cascaded multilevel inverter with different values of dc voltage sources. The main disadvantage of the cascaded multilevel inverter is the high number of required insulated dc voltage sources because each basic unit consists of minimum one dc voltage sources. In addition, high numbers of power electronic devices is used if the magnitude of these dc voltage sources be same [8]. Up to now, several capacitor based multilevel inverters have been presented in literature. In [9], one capacitor is used as one of the required dc voltage sources and the others are insulated dc source. The main disadvantage of this inverter is high number of used dc voltage sources and power electronic devices to generate specific numbers of output levels. In [10], the other capacitor based multilevel inverter has been presented. In this topology, two capacitor and one dc voltage source are used in each basic unit that not only increase the number of used capacitors but also does not decrease the number of used dc voltage sources. Two other capacitor based multilevel inverters have been presented in [11-12]. The main disadvantage of these inverters is the low value of their dc voltage sources that leads to high number of required power electronic devices.

One of the main parameters in operation of the multilevel inverters is their control method. The control methods of multilevel inverters are classified into three major groups: high switching frequency; mixed switching frequency and fundamental switching frequency. In the first control method, the high switching frequency leads to decrease the generated lower order harmonics, volume and size of the filter but increases the switching losses. Space vector PWM, phase shifted PWM and level shifted PWM are three main categories of the high frequency control method. Hybrid PWM (H-PWM) is the other control method based on the mixed switching frequency. In this control method, the switching frequencies of all units are

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different. The fundamental switching frequency control method as a last control method of the multilevel inverter includes of selective harmonic elimination and space vector control methods that is mostly applied in the cascaded multilevel inverters [13-15]. In this control method, the switching frequency is low that leads to decrease the switching losses and increase the efficiency. The main disadvantage of this method is increasing lower order harmonics that causes to increase the size and cost of the filter. In addition, in this control method, the time intervals of using dc voltage sources in all units are differ and because of series connection of units, the power drawn from them will be differ that leads to increase the maintenance cost of the inverter. As a result, charge balance control methods have been presented in [16] but it is impossible to use these control methods for asymmetric cascaded multilevel inverters and capacitor based multilevel inverters.

In this paper, a new capacitor based basic unit is proposed. By series-connected n numbers of proposed basic units, two new cascaded multilevel inverters are proposed. In addition, to generate all voltage levels (even and odd) at the output, three different algorithms to determine the magnitude of dc voltage sources are proposed. Then, the proposed topologies are compared to several conventional capacitor based cascaded multilevel inverters to investigate the advantages and disadvantages of these new proposed topologies. Moreover, because of using capacitors in the proposed topologies and the importance of their voltage balancing, a new control method is proposed. Finally, the accuracy performance of the proposed cascaded inverters is verified through experimental and simulation results.

2. PROPOSED TOPOLOGY

The proposed basic unit is shown in Fig. 1 [17]. As shown in this figure, this basic unit consists of two series-connected inverter legs. Each inverter leg includes of two unidirectional power switches from voltage point of view and one voltage source. The used voltage sources are either an insulated dc voltage source or a capacitor source. Each unidirectional switch consists of one IGBT with an anti-parallel diode with capability of blocking voltage in one direction and conducting current in both directions. Table 1 shows the generated output voltage levels based on different switching patterns. In this Table, 1 and 0 indicate the on and off states of the switches, respectively. As shown in Table 1, the capacitor basic unit is able to generate three voltage levels of V_{dc}, 0 and $-V_C$ at the output. It is important to note that the capacitor can also be used in the downer leg of the proposed capacitor basic unit. In this condition, the proposed basic unit is able to generate three voltage levels of $-V_{dc}$, 0 and $-V_C$ at the output. In addition, in each switching pattern one power switches from each leg (S_{a1} or S'_{a1}) and (S_{a2} or S'_{a2}) are turned on simultaneously to avoid short circuit in voltage side. In other word, in the proposed unit, the used power switches in each inverter leg act complementary. Moreover, in order to generate staircase output voltage with the same steps, the voltage of the capacitor has to be maintained at the constant value of $V_C = V_{dc}$.

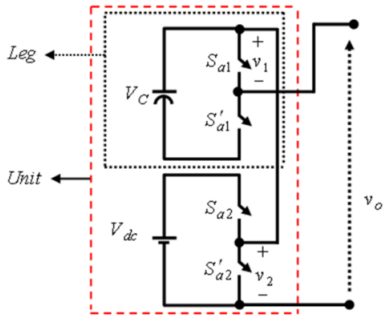


Fig.1: *The proposed capacitor basic unit.*

Table 1: *The Output Voltage of the Proposed Capacitor Basic Unit Based on Different Switching Patterns.*

State	S_{a2}	S'_{a2}	S_{a1}	S'_{a1}	V_o
1	1	0	1	0	V_{dc}
2	1	0	0	1	0
	0	1	1	0	
3	0	1	0	1	$-V_C$

A new-cascaded multilevel inverter can be made by series-connected n numbers of the proposed capacitor basic units. This inverter is shown in Fig. 2. As mentioned before, based on the places of the capacitor, two different cascaded multilevel inverters are proposed. Fig. 2(a) shows the proposed cascaded multilevel inverter that all basic units are same and the capacitor is used only in the second leg of each unit. Fig. 2(b) shows the other proposed cascaded multilevel inverter that the location of the capacitor is substituted between the first and second leg of each unit.

According to Fig. 2, the output voltage of the proposed inverter is equal to add the output levels of different units and is given by:

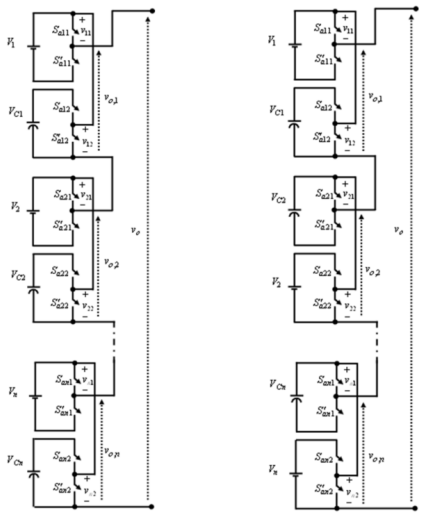
$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \cdots + v_{o,n}(t) \qquad (1)$$

In the proposed cascaded inverters, the number of switches (N_{switch}), IGBTs (N_{IGBT}), driver circuits (N_{driver}), dc voltage sources ($N_{sources}$) and capacitors ($N_{capacitor}$) are calculated as follows:

$$N_{switch} = N_{IGBT} = N_{driver} = 4n \qquad (2)$$

$$N_{source} = n \qquad (3)$$

$$N_{capacitor} = n \qquad (4)$$



(a) (b)

Fig.2: *The proposed cascaded multilevel inverter; (a) with the constant place of the capacitor; (b) different location of the capacitor.*

The other main parameter in calculation the total cost of the inverter is the maximum amount of blocked voltage by the switches. If the values of the blocked voltage by switches are reduced, the total cost of the inverter will be decreased [16]. Therefore, in order to calculate this index, it is necessary to consider the amount of the blocked voltage by each of the switches. According to Fig. 2, the values of the blocked voltage by switch $S_{a,11}$ and $S'_{a,11}$ are equal to:

$$V_{S_{a,11}} = V_{S'_{a,11}} = V_1 \tag{5}$$

In (5), $V_{S_{a,11}}$ and $V_{S'_{a,11}}$ indicate the values of the blocked voltage by the switches $V_{S_{a,11}}$ and $V_{S'_{a,11}}$, respectively. The values of the blocked voltage by switches $V_{S_{a,12}}$ and $V_{S'_{a,12}}$ are equal to:

$$V_{S_{a,12}} = V_{S'_{a,12}} = V_{C1} \tag{6}$$

In (7), $V_{S_{a,12}}$ and $V_{S'_{a,12}}$ indicate the values of the blocked voltage by the switches $V_{S_{a,12}}$ and $V_{S'_{a,12}}$, respectively.

Therefore, the maximum amount of the blocked voltage by all of the used switches in the first unit ($V_{block,1}$) is equal to:

$$V_{block,1} = 2(V_1 + V_{C1}) \tag{7}$$

Similarly, the maximum value of the blocked voltage by the switches in other units is calculated and so the maximum amount of the blocked voltage in the proposed cascaded inverter (V_{block}) is equal to:

$$\begin{aligned} V_{block} &= V_{block,1} + V_{block,2} + \cdots + V_{block,n} \\ &= 4(V_1 + V_{C1} + V_2 + V_{C2} + \cdots + V_n + V_{Cn}) \end{aligned} \tag{8}$$

It is important to note that the magnitude of used dc voltage sources has most important influence in the number of generated output levels and the value of the capacitance. Therefore, in order to generate all positive and negative levels at the output three different algorithms are proposed. According to each proposed algorithm the number of output voltage levels (N_{level}), the maximum amplitude of the producible output voltage ($V_{o,\max}$) , the variety of the value of dc voltage sources ($N_{variety}$) and the maximum amount of the blocked voltage by switches (V_{block}) will be differ. These proposed algorithms and all of the abovementioned indexes are calculated and shown in Table 2. It is important to note that in this Table V_j is the dc voltage source of the i^{th} basic unit and V_{Cj} is its capacitor source while j is considered as $j = 1, 2, \cdots, n$. In addition, all of the proposed algorithms and their obtained results can be used in both proposed cascaded multilevel inverters.

Table 2: *The Proposed Algorithms And Obtained Parameters In The Proposed Cascaded Inverters.*

Proposed algorithms	First proposed algorithms	Second proposed algorithm	Third proposed algorithm
V_j	V_{dc}	$V_1 = V_{dc}$, $V_{j+1} = 2V_{dc}$	$2^{j-1}V_{dc}$
V_{Cj}	V_{dc}	V_j	V_j
N_{level}	$2n+1$	$4n-1$	$2^{n+1}-1$
$V_{o,\max}$	nV_{dc}	$(2n-1)V_{dc}$	$(2^n-1)V_{dc}$
$V_{blocked}$	$4nV_{dc}$	$4(2n-1)V_{dc}$	$4(2^n-1)V_{dc}$
$N_{variety}$	1	2	n

3. PROPOSED CONTROL METHOD

The proposed control method for these new cascaded multilevel inverters is based on the capacitors charging and discharging. The proposed control method is completely analyzed for the shown new topology in Fig. 3.

As shown in this figure, this inverter consists of two basic units that its capacitors are substitute in different inverter leg (according to Fig. 2(b)). In addition, the first proposed algorithm is considered to determine the magnitude of its dc voltage sources. According to Fig. 3, the output voltage of the upper inverter leg of the first basic unit (V_{11}) is equal to zero by turning on the switch S_{a11} and is equal to V_{dc} by turning on the switch S'_{a11}. In the lower inverter leg of the first basic unit, the output voltage (V_{12}) is equal to zero by turning on the switch S'_{a12} and is equal to V_{C1} by turning on the switch S_{a12}. There are the same explanations for the second basic unit. In other word, in the second basic unit, the output voltage of

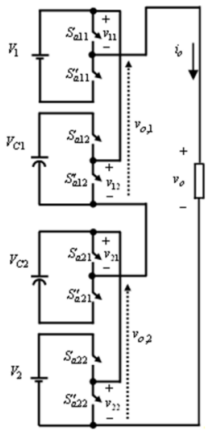


Fig.3: *The proposed cascaded multilevel inverter with two basic units.*

upper inverter leg (V_{21}) is equal to zero by turning on the switch S_{a21} and is equal to V_{C2} by turning on the switch $S^{'}_{a21}$ while in the lower inverter leg V_{22}, its output is equal to V_{dc} when the switch S_{a22} is turned on and is equal to zero when the switch $S^{'}_{a22}$ is turned on. Table 3 shows the output voltage of the first and second basic unit and the inverter's output voltage of the proposed topology that is shown in Fig. 3. As mentioned before, in order to generate staircase output levels with the same steps and according to Table 2, the voltage of the capacitors have to be maintained at the value of $V_{C1} = V_{C2} = V_{dc}$. Therefore, as shown in Table 3, this inverter is able to generate five levels of $+V_{dc}$, $+2V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$ at the output. Fig. 4 shows the generated output voltage waveforms of the proposed inverter.

As shown in Fig. 4 and Table 3, there are two different switching patterns to generate voltage level of $+V_{dc}$ and $-V_{dc}$, which they can be used for charging the capacitors. The voltage level of $+V_{dc}$ is generated either when the switch S_{a22} is turned on and the output voltage of other inverter legs are zero or while the switch S_{a12} is turned on and the output voltage of other inverter legs are zero. This state leads to generate the voltage level of and charge the capacitor of C_1. Therefore, one of these two states is selected based on the output voltage, the current direction and kind of the load. Moreover, there is the same explanation to generate voltage level of $-V_{dc}$ that is indicated in Table 3.

It is important to note that most of the industrial loads are as resistive-inductive load. In this kind of loads, there are phase shift between current and voltage waveforms. It means that in a time interval, the output voltage is positive while the output current is negative that leads to balance the capacitors voltage. The output voltage and current of the considered inverter in Fig. 3 is shown in Fig. 5. As shown in this figure, for instance in the time interval of (t_0, t_1) the output voltage is positive while its current is negative, so, the load current is toward to the capacitor and it is charged. The control method of the proposed inverter to charge and discharge of the capacitors is completely analyzed in the next sub-section.

Table 3: *Output Voltage of the Presented Topology in Fig. 3.*

states	turned on switches	$V_{o,1}$	$V_{o,2}$	V_o
1	$S_{a11}, S_{a12}, S_{a21}, S^{'}_{a22}$	V_{C1}	0	$+V_{dc}$
	$S_{a11}, S^{'}_{a12}, S_{a21}, S_{a22}$	0	$+V_{dc}$	
2	$S_{a11}, S_{a12}, S^{'}_{a21}, S^{'}_{a22}$	V_{C1}	$+V_{dc}$	$+V_{dc} + V_{C1}$
3	$S_{a11}, S^{'}_{a12}, S_{a21}, S^{'}_{a22}$	0	0	0
	$S^{'}_{a11}, S_{a12}, S^{'}_{a21}, S_{a22}$	0	0	
4	$S^{'}_{a11}, S^{'}_{a12}, S_{a21}, S^{'}_{a22}$	$-V_{dc}$	0	$-V_{dc}$
	$S_{a11}, S^{'}_{a12}, S^{'}_{a21}, S_{a22}$	0	$-V_{C2}$	
5	$S^{'}_{a11}, S_{a12}, S^{'}_{a21}, S^{'}_{a22}$	$-V_{dc}$	$-V_{C2}$	$-V_{dc} - V_{C2}$

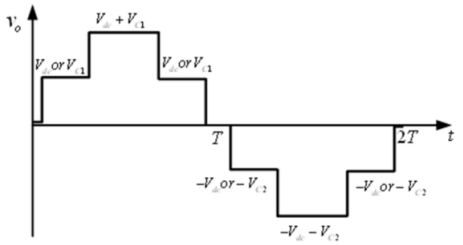


Fig.4: *The output voltage waveform of the proposed cascaded multilevel inverter with two basic units.*

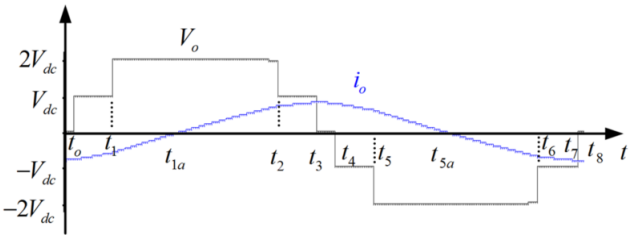


Fig.5: *Output voltage and current waveforms of the proposed cascaded multilevel inverter with two basic units.*

As mentioned in the previous section, there are suitable states for charging the capacitors C_1 and C_2 based on the load current waveform. As it is obvious from Fig. 5, in the time interval of (t_0, t_1), the output voltage is positive while its current is negative. This means that, in this time interval, the direction of the load current is toward to the capacitor. As a result, by turning on the switch S_{a12} the voltage level of $+V_{dc}$ is generated at the output and the capacitor C_1 is charged. This state is shown in Fig. 6(a). In the time interval of (t_2, t_3) that is shown in Fig. 6(b), the output voltage and current are positive. This means that the current direction is toward to the load, therefore, the voltage level of $+V_{dc}$ is generated when the switch S_{a22} is turned on. In this

condition, it is impossible to charge the capacitor. There are the same explanation to generate voltage level of $-V_{dc}$. As shown in Fig. 5, in the time interval of (t_4, t_5), the output voltage is negative while the output current is positive. In this condition, the direction of the output current is changed toward to the capacitor. Therefore, by turning on the switch S'_{a21}, the output voltage will be equal to $-V_{dc}$ and the capacitor of C_2 is charged. This state is shown in Fig. 6(c). In the time interval of (t_6, t_7) that is shown in Fig. 6(d), the output voltage and current are negative, so, the voltage of $-V_{dc}$ is generated and it is impossible to charge the capacitor of C_2. This state is made when the switch S'_{a11} is turned on. The time of charging and discharging of the capacitors in the proposed cascaded inverters according to the Fig. 5 are summarized in Table 4.

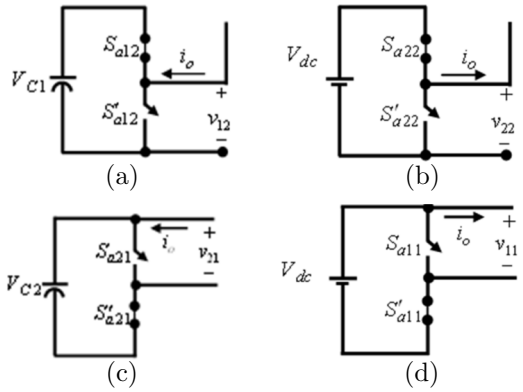


Fig.6: *Output voltage and current polarities of the proposed cascaded multilevel inverter with two basic units in different time intervals; (a) (t_0, t_1); (b) (t_2, t_3); (c) (t_4, t_5); (d), (t_6, t_7).*

Table 4: *The preferred solutions of ZDT problems.*

Time interval	System status	V_0	Capacitor states
$0 \le t < t_0$	$V_o = 0, i_o < 0$	0	constant
$t_0 \le t < t_1$	$V_o > 0, i_o < 0$	V_{C1}	Charging of C_1
$t_1 \le t < t_{1a}$	$V_o > 0, i_o < 0$	$2V_{dc}$	Charging of C_1
$t_{1a} \le t < t_2$	$V_o > 0 i_o > 0$	$2V_{dc}$	Charging of C_1
$t_2 \le t < t_3$	$V_o > 0 i_o > 0$	V_{dc}	constant
$t_3 \le t < t_4$	$V_o = 0 i_o > 0$	0	constant
$t_4 \le t < t_5$	$V_o < 0 i_o > 0$	$-V_{C2}$	Charging of C_2
$t_5 \le t < t_{5a}$	$V_o < 0 i_o > 0$	$-2V_{dc}$	Charging of C_2
$t_{5a} \le t < t_6$	$V_o < 0 i_o < 0$	$-2V_{dc}$	discharging of C_2
$t_6 \le t < t_7$	$V_o < 0 i_o < 0$	$-V_{dc}$	constant
$t_7 \le t < t_8$	$V_o = 0 i_o < 0$	0	constant

It is pointed out that in order to charge the capacitors suitably, it is better to determine the maximum and minimum voltage values of them ($V_{\min} < V_C < V_{\max}$). For instance, in order to generate voltage level of $+V_{dc}$ and charge the capacitor C_1, the switching pattern is selected as follows:

$$If \begin{cases} +0.2V_{dc} \le ref \le +V_{dc} \\ i_o < 0 \\ V_{C1} < V_{\min} \end{cases} then \begin{cases} S_{a12}=1 \\ S_{a11}=S_{a21}=1, S_{a22}=0 \end{cases} \quad (9)$$

In (5), (ref) is the sinusoidal reference signal that is equal to:

$$ref = m \sin(\omega t + \phi) \quad (10)$$

In (6), ϕ is the phase shift of the reference signal and is the magnitude of this signal.

When the capacitor C_1 has been charged to the value of $+V_{dc}$, in order to avoid increasing its voltage value the below limitations are considered:

$$If \begin{cases} +0.2V_{dc} \le ref \le +V_{dc} \\ i_o < 0 \\ V_{C1} > V_{\max} \end{cases} then \begin{cases} S_{a12}=0 \\ S_{a11}=S_{a21}=1, S_{a22}=0 \end{cases} \quad (11)$$

The performance of the proposed control method based on (5) and (7) to generate voltage level of $+V_{dc}$ is shown in Fig.7. Otherwise, as shown in Fig. 6(b) in the time interval of (t_2, t_3), the capacitor of C_1 cannot be charged and the voltage level of $+V_{dc}$ is obtained as follows:

$$If \begin{cases} +0.2V_{dc} \le ref \le +V_{dc} \\ i_o > 0 \end{cases} then \begin{cases} S_{a22}=1 \\ S_{a11}=S_{a21}=1, S_{a12}=0 \end{cases} \quad (12)$$

It is important to note that the control method to generate other voltage levels is as same as the above mentioned explanations.

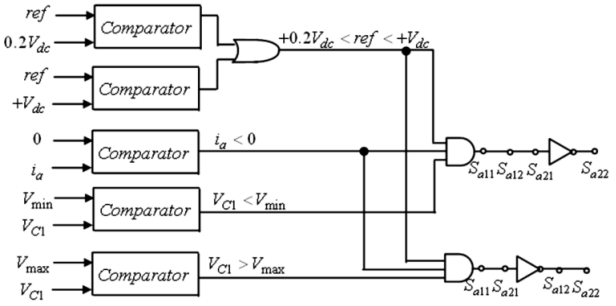


Fig.7: *Proposed control method to generate voltage level of $+V_{dc}$ and charge of the capacitor C_1.*

4. COMPARING THE PROPOSED TOPOLOGY WITH THE CONVENTIONAL TOPOLOGIES

The main aim of proposing the new capacitor based cascaded multilevel inverter is increasing the number of generated output voltage levels by using lower number of power electronic devices. In order to investigate the performance of the proposed topology, a comparison is done between the proposed cascaded multilevel inverter based on its three proposed algorithm with the several conventional capacitor based cascaded multilevel inverters. These comparisons are based on the number of required dc voltage sources,

switches and the capacitors. In addition, the amount of blocked voltage by switches and the variety of the value of used dc voltage sources are also considered in this comparison. The proposed capacitor based topology with its three algorithms that is shown in Fig. 2(a) is considered by $P_1 - P_3$, respectively.

In [9], a cascaded multilevel inverter based on capacitor has been presented. This topology is as same as the H-bridge multilevel inverter with this difference that a capacitor is used as one of the dc voltage sources. As a result, this topology consists of minimum two bridges in which it includes of one dc voltage source and one capacitor. There are two algorithms to determine the magnitude of used dc voltage sources in this topology that are considered by R_1 and R_2 in this comparison. The other capacitor based cascaded multilevel inverter has been presented in [10]. In this topology, there are two capacitors in each bridge which are series-connected. This topology with its algorithm is considered by R_3 in this comparison. In addition, two other capacitor based multilevel inverter have been presented in [11-12]. These topologies consist of only one dc voltage source and n numbers of capacitors. These topologies are considered as R_4 and R_5, respectively. These inverters are shown in Fig. 8.

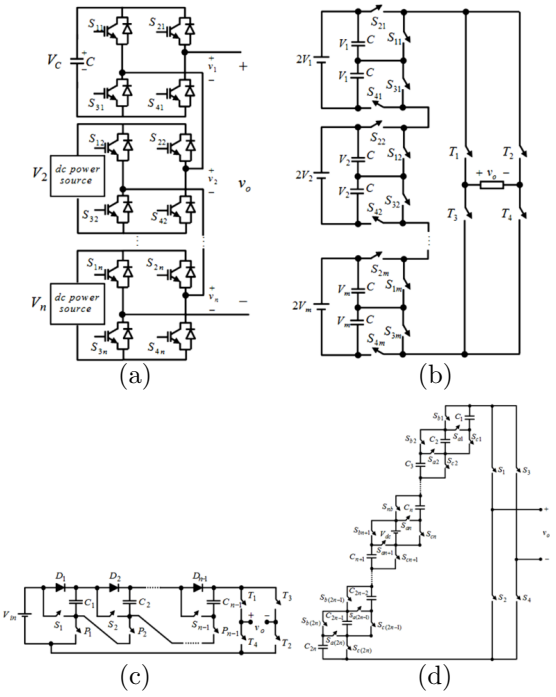


Fig.8: *The capacitor based multilevel inverters; (a) presented topology in [9] (R_1) for $V_C = V_{dc}, V_j = 2V_{dc}$ $j = 1, 2, \cdots, n$, (R_2) for $V_C = V_{dc}, V_j = 3V_{dc}$ $j = 1, 2, \cdots, n$; (b) presented topology in [10] (R_3) for $V_1 = 2V_{dc}, 2V_{dc}, \ldots, V_m = 2V_{dc}$; (c) presented topology in [11] (R_4) for $V_{in} = V_{dc}$; (d) presented topology in [12] (R_5) for $V_{in} = V_{dc}$.*

Fig. 9 shows the number of used switches in the proposed topology in comparison with the other above mentioned multilevel inverters. As shown in this figure, the proposed topology based on its third proposed algorithm needs lower number of power switches. The unidirectional power switches are used in the proposed topology as same as other considered multilevel inverters in this comparison. According to the structure of the unidirectional power switches that are mentioned before, the number of used IGBTs, diodes and driver circuits are also compared in Fig. 9. According to Fig. 9, the proposed capacitor based inverter needs lower number of these components in comparison with the other above mentioned topologies.

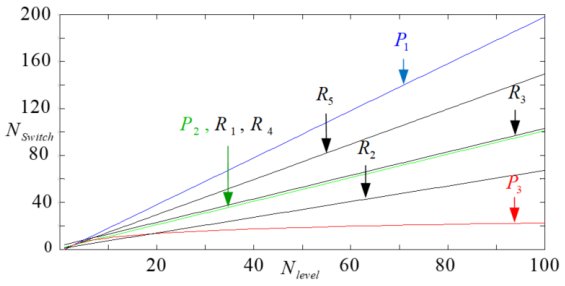


Fig.9: *Variation of N_{switch} versus N_{level}.*

Fig. 10 compares the number of the required dc voltage sources in the proposed topology and the conventional capacitor based multilevel inverters. The proposed topology needs lower number of dc voltage sources in comparison with other above mentioned inverters except R_4 and R_5. This is due to use only one dc voltage source in the topologies presented as R_4 and R_5. In addition, this advantage of the proposed topology is remarkable especially when the third proposed algorithm is used for.

Fig. 11 compares the number of the required capacitors in the proposed topology and the other above mentioned multilevel inverters. The proposed topology needs lower number of capacitors in comparison with other inverters except R_1 and R_2. This is due to use only one capacitor in the presented topology as R_1 and R_2. In addition, the considered inverters as R_4 and R_5 that only one dc voltage source is used in their topologies need higher number of capacitors in comparison with the proposed topology.

The comparison of the value of the generated blocked voltage by power switches in the proposed topologies with other capacitor based inverters is shown in Fig. 12. As shown in this figure, the proposed inverter has minimum value of the blocked voltage in comparison with the other above mentioned topologies. Fig. 13 compares the variety of the value of dc voltage sources. As shown in this figure, the proposed topology based on the first proposed algorithm has better performance in relation to the others.

It is resulted that the proposed topology based on

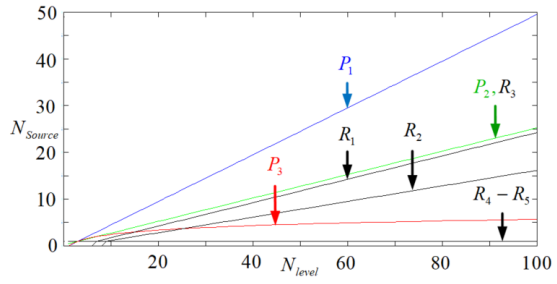


Fig.10: *Variation of* N_{source} *versus* N_{level}.

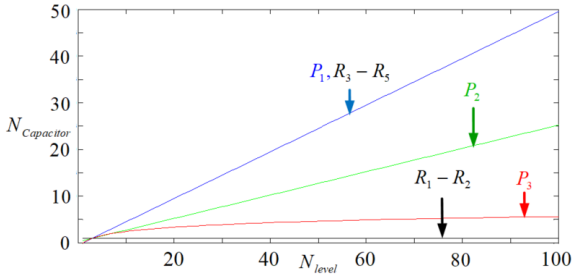


Fig.11: *Variation of* $N_{capacitor}$ *versus* N_{level}.

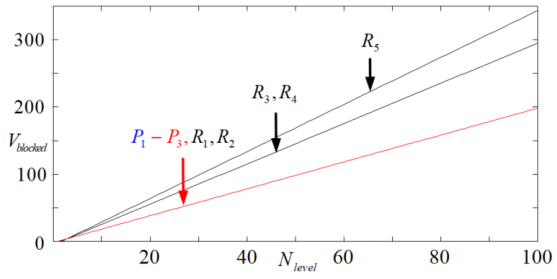


Fig.12: *Variation of* $N_{blocked}$ *versus* N_{level}.

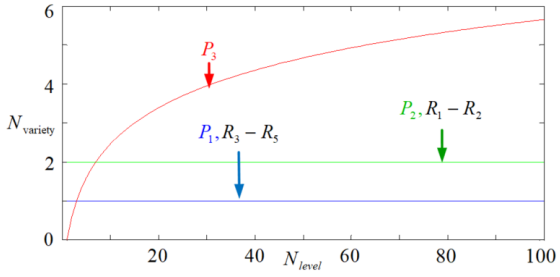


Fig.13: *Variation of* $N_{variety}$ *versus* N_{level}.

three algorithms needs minimum number of power electronic devices. In addition, these topologies need lower number of dc voltage source and capacitors in comparison to the others. It is important to note that, in some topologies only one dc voltage source is used and in some of them only one capacitor is used. Therefore, the other advantage of the proposed topology is the same numbers of required dc voltage sources and capacitors that lead to decrease the starting and maintenance cost of the inverter. In addition, the proposed inverter generates lower amount of the blocked voltage by the power switches. This is the other advantage of the proposed capacitor based topology. It is important to note that all obtained results are also as same as the other proposed topology that is shown in Fig. 2(b).

5. SIMULATION RESULTS

In order to verify the accuracy performance of the proposed capacitor based cascaded multilevel inverter to generate all voltage levels at the output, simulation results in EMTDC/PSCAD software program are used. The proposed cascaded inverter is shown in Fig. 3. As shown in this figure, this inverter consists of two proposed basic units, eight unidirectional power switches, two dc voltage sources and two capacitors. The first proposed algorithm is considered to determine the magnitude of voltage sources. According to obtained equation in Table 2, the voltage values of dc sources and capacitors are equal to $V_1 = V_2 = V_{dc}$ and $V_{C1} = V_{C2} = V_{dc}$, respectively. In addition, based on the equations of the maximum number and amplitude of output levels from Table 2, this inverter has to be able to generate five levels (two positive, two negative and one zero levels) with the maximum amplitude of $440V$ at the output if $V_{dc} = 110V$. The capacitance of each capacitor is considered $C = 1000\mu F$. In all process of the simulation performance, the load is assumed as resistive-inductive load $(R - L)$ with the magnitudes of $R = 13\Omega$ and $L = 200mH$. In this paper, the proposed control method that is completely mentioned in section 3 is used.

Fig. 14 shows the output voltage of each inverter leg. As shown in Figs. 14(a) and 14(d), the maximum output voltage of the first and second inverter legs is equal to $110V$. In addition, based on the Figs. 14(b) and 14(c), the capacitors voltage of these inverters legs are maintained in the value of V_{dc} that is equal to $110V$. In other word, by considering the first proposed algorithm, the capacitors voltage are maximally charged to the value of V_{dc} but if the second proposed algorithms is considered, the capacitors will be charged to the voltage value of $2V_{dc}$.

The output voltage and current waveforms of the proposed cascaded inverter are shown in Fig. 15. As shown in Fig. 15(a), the proposed inverter is able to generate five levels by using capacitors and dc voltage sources with the maximum amplitude of $220V$ at the output. This result is obtained by using suitable control method to charge and discharge the capacitors. By comparing Figs. 15(a) and 15(b), it is clear that the current waveform is near to ideal sinusoidal waveform than voltage waveform and there is a phase shift between voltage and current waveforms. These differences are made because of the resistive-inductive load feature that acts as a low pass filter.

In this simulation, in order to balance the ca-

pacitors voltage and generate desirable output levels, their maximum and minimum voltage values are selected as $240V$ and $200V$, respectively. The output voltage waveforms of the capacitors are shown in Figs. 16(a) and 16(b), respectively. As shown in these figures, the capacitors voltage of C_1 and C_2 are increased from their initial value that is equal to zero to its maximum value that is equal to $V_{dc} = 220V$. These figures also show that the variation of the capacitors voltage from starting to steady state takes $t = 0.8sec$ and after this time they will be maintained at the constant values.

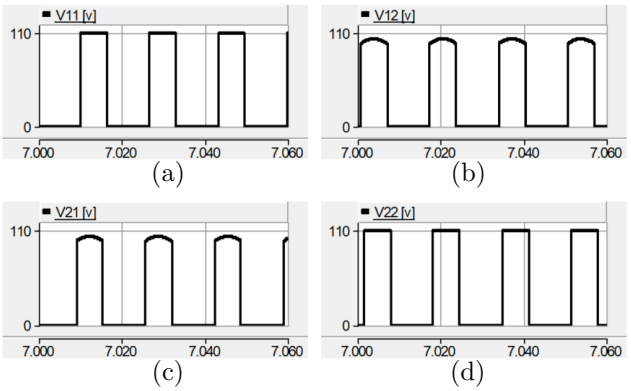


Fig.14: *Output waveforms of the proposed five-level inverter; (a) output voltage; (b) output current.*

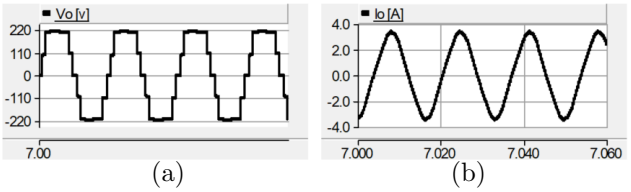


Fig.15: *Output waveforms of the proposed five-level inverter; (a) output voltage; (b) output current.*

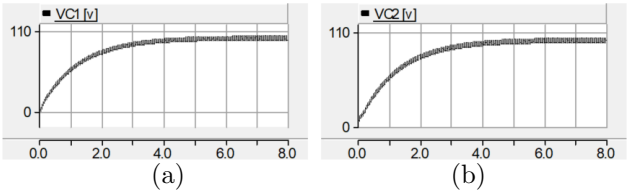


Fig.16: *The capacitors output voltages; (a) voltage across C_1 from starting to steady state; (b) voltage across C_2 from starting to steady state.*

6. EXPERIMENTAL RESULTS

To prove the correct operation of the proposed topology and control method, the proposed topology that is shown in Fig. 3 is implemented in laboratory in the same conditions with the simulation. Fig. 17 shows the experimental results. As shown in this figure, there is a good agreement between the simulation and experimental results. There is a small difference in amplitudes due to using real components in practice.

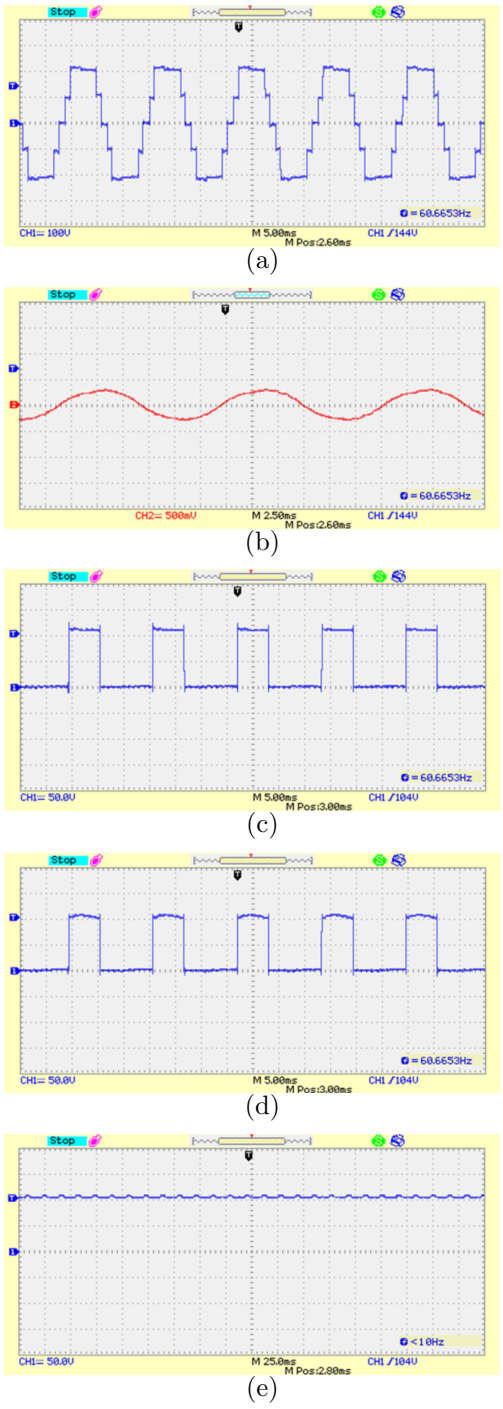


Fig.17: *Experimental results; (a) output voltage; (b) output current; (c) voltage across switch S'_{a11}; (d) voltage across switch S'_{a12}; (e) voltage across C_1 in steady state condition.*

7. CONCLUSIONS

In this paper, a new capacitor basic unit is proposed. By using n numbers of the proposed basic units, two kinds of cascaded multilevel inverters are proposed. The main difference between these two kinds of inverter is related to the location of the capacitors in the basic unit. In order to generate even and odd voltage levels at the output, three different algorithms are proposed. Minimum number of used switches, IGBTs, diodes and driver circuits are the main advantages of the proposed topologies in comparisons with the many of the presented capacitor based multilevel inverters. In addition, the proposed topologies need lower number of dc voltage source and capacitors in comparison with the others. These are due to consider the same number of required dc voltage sources and capacitors in the proposed topologies that lead to decrease the starting and maintenance cost of the inverter. In addition, by considering the structure of the proposed topologies and their algorithms, the proposed inverters generate lower amount of blocked voltage by the power switches. This is the other advantage of the proposed capacitor based topologies. In this paper, Moreover, a new control method to balance the capacitors voltage and generate all voltage levels is proposed. At the end, a five-level inverter based on first proposed algorithm and proposed control method are simulated in EMTDC/PSCAD program to reconfirm the ability of the proposed topology and its new control method in generating all (even and odd) output voltage levels. Moreover, to prove the performance of the proposed topology, the experimental results are given.

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