Output Voltage Control of the SP Topology IPT System based on a Primary Side Controller Operating at ZVS

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ABSTRACT

This paper presents a technique to control the output voltage of a series-parallel (SP) topology inductive power transfer (IPT) system using only a controller, located on the primary side. This reduces the cost, size, complexity and loss of the system compared to conventional IPT dual-side controllers. An asymmetrical duty cycle control (ADC) of full-bridge inverters was used to control the DC output voltage to its designed value. Additionally, a zero voltage switching (ZVS) operation can be obtained at all power levels by varying the switching frequency of the inverter. Theoretical analysis was performed through a mutual inductance coupling model and verified by computer simulation. Experimental results of the circular magnetic structure IPT system with an adjustable air-gap confirm the validity of the proposed controller. The system efficiency was improved throughout the operation and the improvement became obvious as the output power was decreased.

Keywords: IPT System, SP Topology, Primary Side Controller, ADC Control, ZVS Operation

1. INTRODUCTION

Recently, an inductive power transfer (IPT) technique has received much interest and has been widely adopted. This technique allows for contactless power transfer from a source to a load over a relatively large air gap via magnetic fields. Due to the use of inductive coupling, there is no direct physical or electrical contact between the electric source and load. This makes them safer and more convenient compared with conventional conductive power transfer. Such a new technology has been used successfully in many applications including a material handling system, public transport system, EV battery charger, consumer electronics and medical implantable devices [1-3]. Fig. 1 shows a typical IPT system. The primary and secondary compensations are used to compensate for the reactive power required by the coils. By doing that, the power transfer capability or system efficiency can be increased. Thus, compensation capacitors may be connected in series (S) or parallel (P) to the primary coil, secondary coil, or both coils. The commonly used compensation topologies are series-series (SS), series-parallel (SP), parallel-series (PS), and parallel-parallel (PP) as illustrated in Fig. 2 [4-6]. Parallel compensation on the primary side as in PP and PS requires an additional inductor to form a current source, which increases the cost and complexity of the system. The key benefits of the SP topology compared with the SS topology are that the inverter current and the voltage stress in the primary capacitor are lower, for the same output voltage [7]. The SP topology was examined in the current work.

To control the DC output voltage of the IPT system, a secondary side controller is required to modulate the switch mode DC-DC converter located on the load side, also known as the conventional IPT dual-side controller [8,9]. This increases the cost, size, complexity, and loss of the system. Also, it may cause excessive heat and therefore cannot be used in some applications such as implantable medical devices [10]. To overcome the aforementioned drawbacks, the output voltage control of the IPT system using only a controller located on the primary side was introduced with SS topology [11-13]. For SP topology, a load variation may result in non-ZVS operation if fixed frequency control is adopted [14]. Powering up from the non-ZVS operation unavoidably affects the inverter efficiency. This is due to the change in the reflected reactance in the primary circuit, related to the primary resonant frequency. Owing to its simple control and easy implementation, ADC control is a common technique chosen for many full-bridge inverters. However, non-ZVS operation may occur during adjustment of the duty cycle of the inverter voltage.

This paper presents an output voltage control method of SP topology IPT systems using only a primary side controller where the variable frequency ADC control of a full-bridge inverter is applied. The DC output voltage can be controlled to its designed

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value by adjusting the duty cycle of the inverter voltage while the ZVS operation is maintained by varying the switching frequency. The removal of the DC-DC converter and controller in the secondary circuit reduces the cost, size and complexity of the system. Its efficiency can be improved over the fixed frequency ADC control. Theoretical analysis of the non-ZVS mode due to load and angle variations was performed and verified by computer simulation and experimental results.

2. THEORETICAL ANALYSIS

Non-ZVS operation due to the load and alpha angle (α) variations was analyzed in this section based on the mutual inductance coupling model of an SP topology IPT system. Additionally, the minimum switching frequency that achieves ZVS operation for a given load resistance and α angle was introduced.

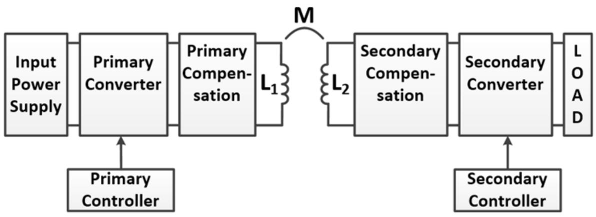

Fig.1: *Typical inductive power transfer (IPT) system.*

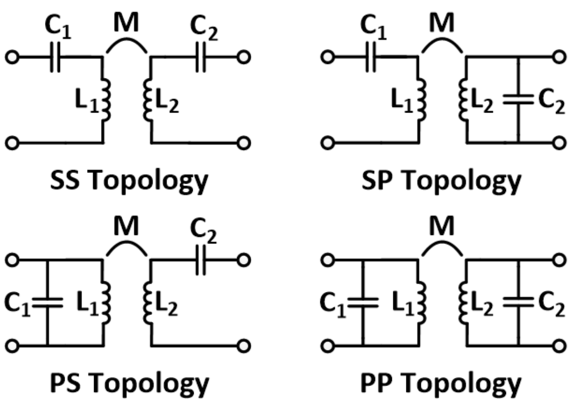

Fig.2: *Commonly used compensation topologies.*

2.1 Mutual inductance coupling model

The commonly used model for an IPT system operating with mutual inductance coupling is illustrated in Fig. 3 (a) [15]. The primary circuit is supplied with a sinusoidal voltage source (V_1). The compensation capacitors, C_1 and C_2, are connected in series with the primary coil and in parallel with the secondary coil, respectively, to form an SP topology. The coupled coil has a mutual inductance, M, and self-inductance values, L_1 and L_2. The winding resistances of both coils are denoted as R_1 and R_2. R_L is the load resistance. The induced voltages in both coils are shown in series with the coil's inductance.

Since $R_2 \ll \omega L_2$, the secondary coil impedance is $\vec{Z}_2 \approx j\omega L_2$. Using the source transformation, the resistance R_2 is combined with the load resistance R_L as,

$$R'_L = \frac{R_L(R_2^2 + X_{L2}^2)}{R_2R_L + (R_2^2 + X_{L2}^2)} \tag{1}$$

The system is transformed from Fig. 3 (a) to 3 (b). At resonant frequency, the load voltage can be obtained by,

$$\vec{Z}_L = \frac{M\vec{I}_1R'_L}{L_2} \tag{2}$$

Thus, the secondary current in Fig. 3 (a) is calculated as,

$$\vec{I}_2 = \frac{j\omega_{02}M\vec{I}_1 - \vec{V}_L}{R_2 + j\omega_{02}L_2} \tag{3}$$

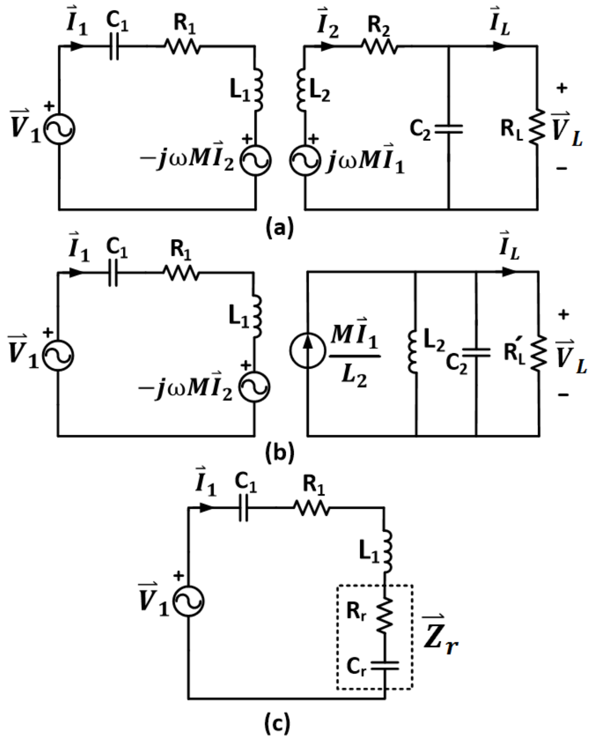

Fig.3: *Mutual inductance coupling model of the SP topology IPT system.*

The reflected impedance referred to the primary circuit can be obtained by dividing the primary induced voltage by the primary current as [15],

$$\vec{Z}_r = \frac{-j\omega_{02}M\vec{I}_2}{\vec{I}_1} \tag{4}$$

Substituting (3) into (4) results in,

$$\vec{Z}_r = \frac{\omega_{02}^2 M^2 (R_2 + R_L') - j\omega_{02} M^2 (\omega_{02}^2 L_2 - R_L' R_2 / L_2)}{R_2^2 + \omega_{02}^2 L_2^2} \tag{5}$$

From (5), the reflected resistance and capacitance which are connected in series with the primary winding as shown in Fig. 3 (c) can be defined in (6) and (7), respectively, as,

$$R_r = \frac{\omega_{02}^2 M^2 (R_2 + R_L')}{R_2^2 + \omega_{02}^2 L_2^2} \tag{6}$$

$$X_{cr} = \frac{\omega_{02} M^2 (\omega_{02}^2 L_2 - R_L' R_2 / L_2)}{R_2^2 + \omega_{02}^2 L_2^2} \tag{7}$$

From Fig. 3 (c), the primary resonant frequency and the reflected capacitance can be calculated as,

$$\omega_{01} = \frac{1}{\sqrt{L_1 \left(\frac{c_1 c_r}{c_1 + c_r} \right)}} \tag{8}$$

and,

$$C_r = \frac{1}{\omega_{02} X_{cr}} \tag{9}$$

From (7)–(9), the load variation affects the value of the reflected capacitance. This causes the primary resonant frequency to change. The ZVS and non-ZVS operating regions are illustrated in Fig. 4. If the switching frequency (fs) is fixed as indicated by the solid line, non-ZVS operation will occur when the load resistance is decreased. This is the case where the switching frequency becomes lower than the primary resonant frequency. In other words, the system will operate in a non-ZVS mode if the load resistance is decreased from its design value of 50 Ω. Additionally, non-ZVS operation is rather sensitive to the reduction of the load resistance and to the incremental magnetic coupling coefficient (k).

2.2 Asymmetrical duty cycle (ADC) control

ADC control is one of the commonly used controls for a full-bridge inverter. Gate signals and output voltage waveforms obtained from the ADC control are shown in Fig. 5. The gate signals V_{G4} and V_{G2} are identical to V_{G1} and V_{G3} signals, respectively. Each pair of switches operates in a complementary manner. Thus, the alpha angle (α) of the inverter output voltage (V_{inv}) is controlled by adjusting the duty cycle (D) of V_{G1}. The amplitude and phase of the fundamental component (v_1) of the inverter output voltage, can be obtained by,

$$\left| \vec{V_1} \right| = \frac{4V_{DC}}{\pi} \cos\left(\frac{\alpha}{2} \right) \tag{10}$$

and

$$\phi_{v1} = \frac{\alpha}{2} \tag{11}$$

where ϕ_{v1} is a phase difference between the inverter voltage and its fundamental component as shown in Fig. 5. Taking the rising edge of an inverter voltage as a reference, the voltage v_1 always leads v_{inv} or $\phi_{v1} \geq 0$. The primary circuit current is represented by i_1, as shown in Fig. 5, where ϕ_{i1} is a phase difference compared with the inverter voltage. From (2) and (10), the relationship between the output voltage (V_L) and the duty cycle (D) of the inverter voltage can be expressed as,

$$\left| \vec{V_1} \right| = \frac{4V_{DC} M R_L' \cos\left[(0.5 - D) \times 180°\right]}{\pi L_2 (R_1 + R_r)} \tag{12}$$

Clearly, the magnitude of the output voltage is at its maximum at D = 0.5 and decreases with the duty cycle. By adjusting the duty cycle, the magnitude of the output voltage can be controlled. From Fig. 3 (c), the input impedance as seen from the voltage source is calculated as,

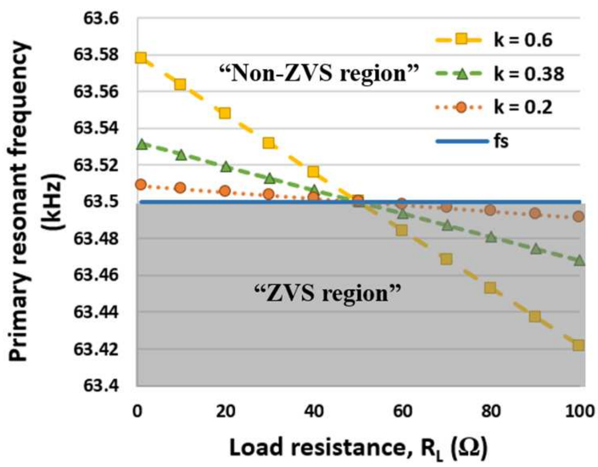

Fig.4: *Non-ZVS operation due to load variation.*

$$\vec{V}_{in} = (R_1 + R_r) + j(X_{L1} - X_{C1} - X_{cr}) \tag{13}$$

The phase angle is obtained by,

$$\theta_{\vec{Z}_{in}} = \tan^{-1} \left(\frac{\mathrm{Im}\{\vec{Z}_{in}\}}{\mathrm{Re}\{\vec{Z}_{in}\}} \right) \tag{14}$$

In a typical operation, most IPT systems are connected with a high quality factor (Q) circuit. The inverter voltage and primary current can be approximated by the fundamental components, (v_1) and (i_1). Thus, ϕ_{i1} can be approximated as,

$$\phi_{i1} = \phi_{v1} - \theta_{\vec{Z}_{in}} \tag{15}$$

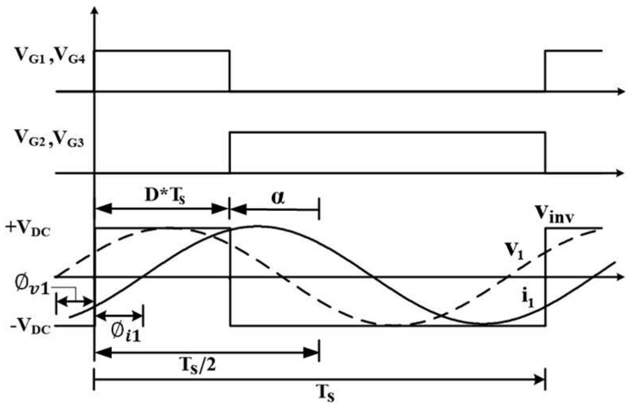

Fig.5: *Gate signals and output voltage waveform of the full-bridge inverter with ADC control.*

In Fig. 5, the condition for ZVS operation is that the primary current lags the inverter voltage or,

$$\phi_{i1} \leq 0 \tag{16}$$

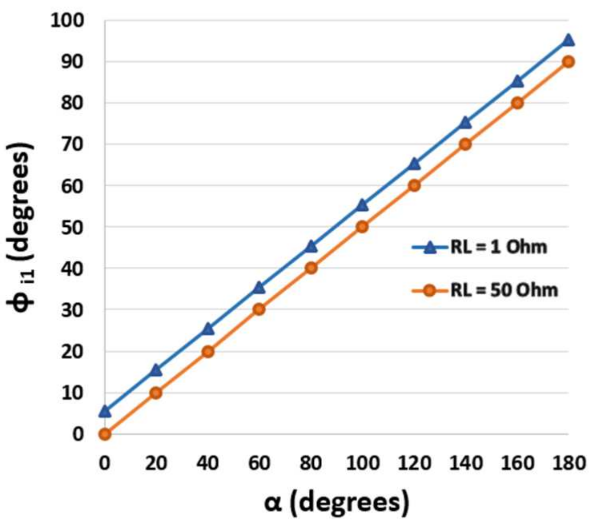

Fig.6: *Non-ZVS operation due to α angle variation.*

A plot of ϕ_{i1} against the α angle is shown in Fig. 6 where the targeted load resistance is 50 Ω. As seen from the plot, the primary current will lead the inverter voltage ($\phi_{i1} > 0$) when the α angle is higher than 0°, which causes non-ZVS operation. The phase difference, ϕ_{i1}, is increased with the α angle. When the load resistance is decreased from its design value, ϕ_{i1} becomes greater than 0° even at $\alpha = 0°$. For a given α angle and load resistance, the minimum switching frequency that achieves the ZVS condition ($\phi_{i1} = 0°$) can be calculated as,

$$f_{s,\min} = \frac{A + \sqrt{A^2 + 4\left\{C_1\left(L_1 - \dfrac{M^2}{L_2}\right)\right\}}}{4\pi\left[C_1\left(L_1 - \dfrac{M^2}{L_2}\right)\right]} \tag{17}$$

and

$$A = \frac{C_1 M^2 R_L \tan\left(\dfrac{\alpha}{2}\right)}{L_2^2} \tag{18}$$

As seen from the plot of $f_{s,\min}$ against α angle in Fig. 7, to maintain ZVS operation, the switching frequency must be increased from the primary resonant frequency after the α angle is increased. The value of $f_{s,\min}$ is increased with the α angle. Moreover, a high load value tends to require a higher switching frequency to achieve ZVS operation.

3. VERIFICATION

To verify the proposed control and analysis, a computer simulation was performed. Fig. 8 shows that the circuit used in the simulation consisted of a DC voltage source, full-bridge inverter, coupled coils, compensation capacitors and a resistive load. The circuit para-

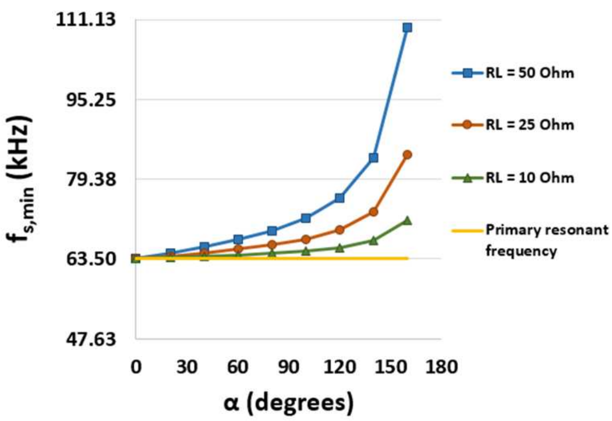

Fig.7: *Minimum switching frequency to achieve a ZVS operation.*

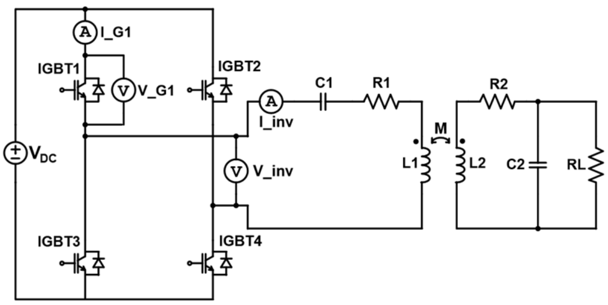

Fig.8: *Simulation circuit.*

meters used in the simulation are listed in Table 1. Simulation waveforms of the IGBT voltage (V_G1), IGBT current (I_G1), inverter voltage (V_inv) and inverter current (I_inv) at various load resistances and α angles are illustrated in Figs. 9–13. In Fig. 9, when the load resistance was at the design value (50Ω) and the α angle was set to 0°, and ZVS operation is achieved. The primary current is essentially in-phase with the inverter voltage causing a phase difference ϕ_{i1} of 0°. Here, the system is operated at its primary resonant frequency. When the load resistance was decreased to 1 Ω while α and f_s remained unchanged, non-ZVS operation occurs as illustrated in Fig. 10. The primary current slightly leads the inverter voltage and ϕ_{i1} becomes positive. This is in agreement with the results shown in Fig. 4. When the α angle was increased from 0° to 90°, non-ZVS operation also occured as illustrated in Fig. 11. This agrees with the results observed in Fig. 6. Fig. 12 depicts non-ZVS operation when RL was decreased from 50Ω to 10Ω and α was increased from 0° to 135°, while f_s was fixed at 63.5 kHz. By increasing the switching frequency to 66.68 kHz, as obtained from (17), the system can be restored so that it operates under a ZVS condition as shown in Fig. 13. This verifies the previous theoretical analysis.

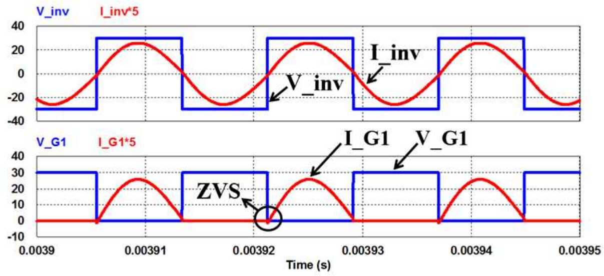

Fig.9: *Simulation results of a ZVS operation (R_L= 50 Ω, α = 0° and f_s = 63.5 kHz).*

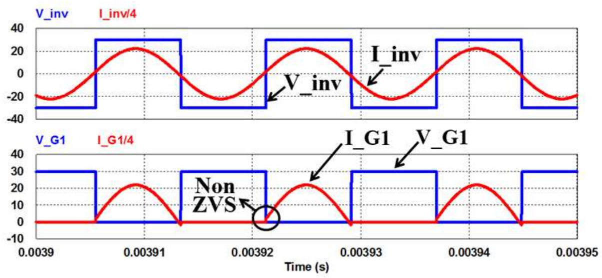

Fig.10: *Simulation results of a non-ZVS operation (R_L= 1 Ω, α = 0° and f_s = 63.5 kHz).*

4. PROPOSED CONTROLLER

From the previous section, non-ZVS operation occurs when the load resistance is decreased from the

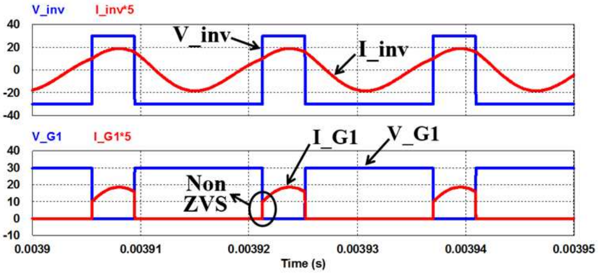

Fig.11: *Simulation results of a non-ZVS operation (R_L= 50 Ω, α = 90° and f_s = 63.5 kHz).*

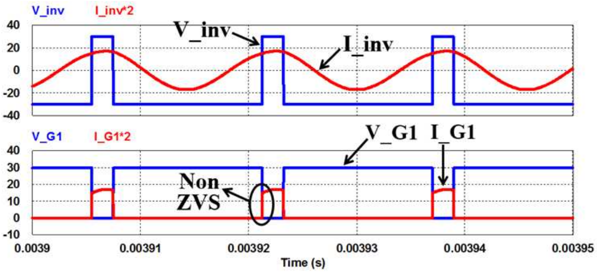

Fig.12: *Simulation results of a non-ZVS operation (R_L= 10 Ω, α = 135° and f_s = 63.5 kHz).*

design value or when the α angle is increased from 0°,

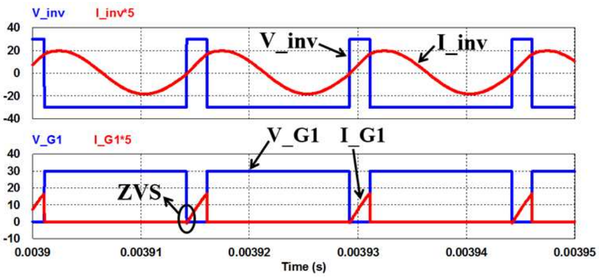

Fig.13: *Simulation results of a ZVS operation (R_L= 10 Ω, α = 135° and f_s = 66.68 kHz).*

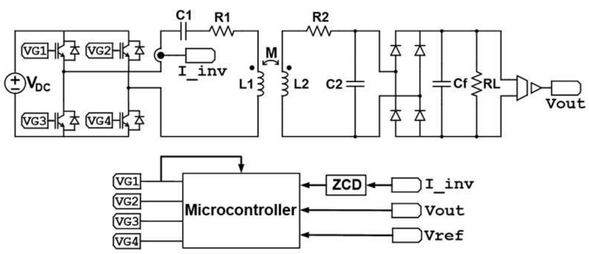

Fig.14: *Overall system of the proposed controller.*

while the system is operated at a fixed frequency. However, by increasing the switching frequency, the inverter is operated in a ZVS mode. Therefore, the controller proposed in this paper is based on a variable frequency control. Fig. 14 shows the overall

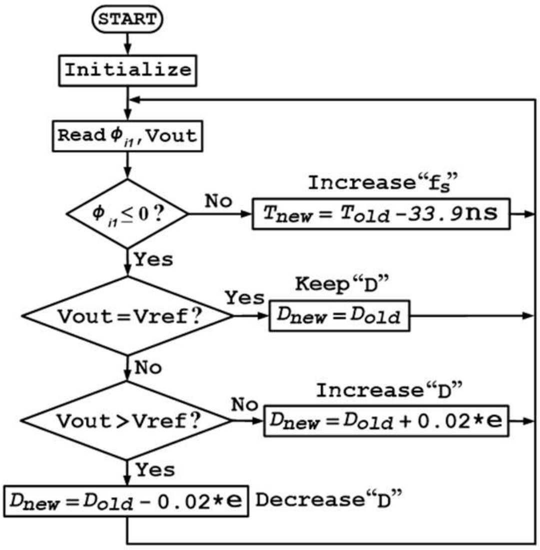

Fig.15: *Flowchart for the microcontroller.*

system of the proposed controller. The primary circuit is supplied by a full-bridge inverter to produce a high frequency voltage. The induced voltage on the secondary side is then modulated using a full-wave rectifier. The aim of the proposed controller is to modulate the DC output voltage at the desired value under a ZVS mode of operation. Variable frequency asymmetrical duty cycle (ADC) control of the full-bridge inverter is used in the proposed method. To regulate the DC output voltage, the α angle of the inverter voltage (V_{inv}) was controlled by adjusting the duty cycle of the gate signal V_{G1}. The switching frequency of the inverter circuit was adjusted for ZVS operation. As shown in Fig. 14, signals fed back to the controller are the DC output voltage (V_{out}), inverter current (I_{-inv}) and gate signal (V_{G1}). The phase of the inverter current was obtained by a zero current detection (ZCD) circuit. The gate signal, VG1, represents the phase of the inverter voltage. The flowchart of the proposed controller is shown in Fig. 15. The phase difference between the inverter voltage and current (ϕ_{i1}) was obtained using an input capture function of the microcontroller. An analog to digital function was used to obtain the value of the DC output voltage (V_{out}). First, a ZVS condition ($\phi_{i1} \leq 0$) was checked. If the system is operating under a non-ZVS mode, the controller will increase the switching frequency until a ZVS mode is achieved. Then, the output voltage condition is checked. If the DC output voltage is lower than the reference voltage (V_{ref}), the controller increases the duty cycle of V_{G1} to increase the output voltage. Alternatively, if the DC output voltage is higher than the reference value, the controller will decrease the duty cycle of V_{G1} to reduce the DC output voltage to the desired value. The process of the duty cycle adjustment stops when the output voltage is equal to the reference voltage.

The steps for duty cycle and switching frequency adjustments, as shown in Fig. 15, are empirically obtained where the optimum response is taken into consideration. The switching period of the inverter is denoted by "T" while "e" is an error from a comparison between the output and reference voltages. Since the primary quality factor (Q_1) is relatively high, its bandwidth is narrow. The change in frequency is very sensitive to the phase difference between the inverter voltage and current (ϕ_{i1}). The minimum step of the switching period variation was chosen as 33.9 ns, which is the smallest achievable step of the selected microcontroller. Larger values of the frequency step may cause an increase in ϕ_{i1}, sacrificing system efficiency and output power. To improve the system response, the change in the step for the duty cycle is dependent on the error (e). A large change step causes an overshoot in the response. If the change step is too small, it may take longer for the response to reach a steady state.

5. EXPERIMENTAL RESULTS

To validate the proposed controller, an experimental setup, as shown in Fig. 16, was implemented. Experiments of output voltage control due to step changes in reference voltage and air gap were performed.

5.1 Design of a coupled coil

The design objective was to send an output power (P_{out}) of 200 Watts to a 20 Ohm load resistance (R_L) with

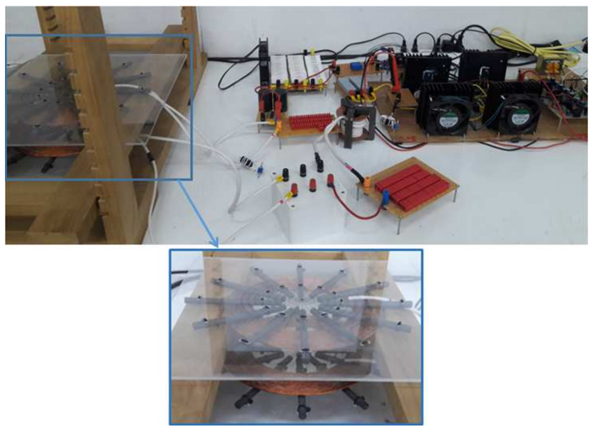

Fig.16: *Experimental setup.*

90% efficiency (η) from a 30 Volt DC (VDC) input with a switching frequency (fs) of 63.5 kHz.
The design constraints were:

1) Primary coil is identical to secondary coil ($L_1 = L_2$ and $R_1 = R_2$).
2) The system is operated at a secondary resonant frequency ($f_s = f_{02}$).
3) The quality factor of the primary circuit was high ($Q_1 > 10$).

Table 1: *Measured circuit parameters with a 6 cm airgap.*

Parameters	**Value**
L_1	104.1 μH
L_2	105.8 μH
M	40.07 μH
k	0.38
R_1	0.25Ω
R_2	0.25Ω

From the design objective and constraints, coupled coils were designed as follows.

At first, the required magnitude of primary current is calculated from,

$$\left|\vec{I}_1\right| = \frac{\pi P_{out}}{2\eta V_{DC}} \tag{19}$$

$$= \frac{\pi(200)}{2(0.9)(30)} = 11.64 \text{ A}$$

From (19), the diameter of a conduction wire is selected for the designed current. The required magnetic coupling can be obtained using the calculated $\left|\vec{I}_1\right|$ as,

$$k = \sqrt{\frac{2P_{out}}{\left|\vec{I}_1\right|^2 R_L}} \tag{20}$$

$$= \sqrt{\frac{2(200)}{(11.64)^2(20)}} = 0.384$$

Next, the minimum value of the primary coil's inductance for a high primary quality factor can be calculated as,

$$L_{1,\min} = \frac{20V_{DC}}{\pi^2 f_{02}\left|\vec{I}_1\right|} \tag{21}$$

$$= \frac{20(30)}{\pi^2(63.5k)(11.64)} = 82.25\ \mu\text{H}$$

The exact value of the coil's inductance is dependent on the air gap. The larger the air gap distance, the greater the inductance needed to achieve the required magnetic coupling. The maximum value of the coil's resistance with a primary quality factor higher than 10 can be obtained using the calculated $L_{1,\min}$ as,

$$R_{1,\max} = \frac{2(P_{out}/\eta - P_{out})}{\left[\left|\vec{I}_1\right|^2 + k^2\left|\vec{I}_1\right|^2(1 - R_L/2\pi f_{02}L_{1,\min})\right]} \tag{22}$$

From (22), the calculated value of $R_{1,\max}$ was 0.31 Ω. From the calculated design values, the coupled coil can be implemented. Due to the advantage of scalable functions, a coupled coil with a circular magnetic structure was used in this study. A ferrite arrangement was selected since it exhibits the highest value of ferrite utilization, as discussed in [16]. A litz-wire made from 50 AWG 31 wires was used as the conduction wire. The primary and secondary coils were identical and consisted of 16 turns of litz-wire. Each coil had 12 pieces of ferrite bars attached, as shown in Fig. 16. The measured circuit parameters at a 6 cm air gap are listed in Table 1. Load resistance used in the experiment was 20 Ω. The secondary resonant frequency was 63.5 kHz. The DC input voltage was maintained at 30 V.

5.2 Output voltage control

Experimental results of the output voltage control under a step change of the reference voltage are shown in Figs. 17–20. For comparison, the results from both fixed and variable frequency ADC controls are shown for both ZVS and non-ZVS operations. Experimental results of the DC output voltage control with a step change in the reference voltage from 63 to 40 V are shown in Figs. 17 and 18, for fixed and variable frequency ADC control, respectively. At the beginning of operation, the DC output voltage was set to 63 V where $\alpha = 0°$ and $f_s = 63.5$ kHz. ZVS operation was achieved since the primary current was in-phase with the inverter voltage as shown in Figs. 17 (b) and 18 (b). Then, the reference voltage was changed to 40 V. The DC output voltage was decreased to 40 V for both fixed and variable frequency ADC control by automatically decreasing the duty cycle of the inverter voltage. In Fig. 17 (c), non-ZVS operation occurred as seen from the leading phase of the inverter current compared with the inverter voltage. In fact, the α angle was greater than 0° and the switching frequency was fixed. However, by the use of the proposed variable frequency ADC control, ZVS operation could be obtained by automatically increasing the switching frequency. This results in a lagging phase of the primary current as shown in Fig. 18 (c). Figs. 19 and 20 show the step response of DC output voltage with a step increase in the reference voltage from 30 to 50 V. At the beginning of operation where DC output voltage was set to 30 V, non-ZVS operation occurred as shown in Figs. 19 (b) and 20 (b). This was due to $\alpha > 0°$ when f_s was fixed at 63.5 kHz. Then, V_{ref} was instantaneously increased to 50 V. The DC output voltage was increased to 50 V by varying the duty cycle of the inverter voltage. Non-ZVS operation was observed in the system with fixed frequency ADC control as shown in Fig. 19 (c). With the proposed variable frequency ADC control, ZVS operation can be obtained by automatically increasing the

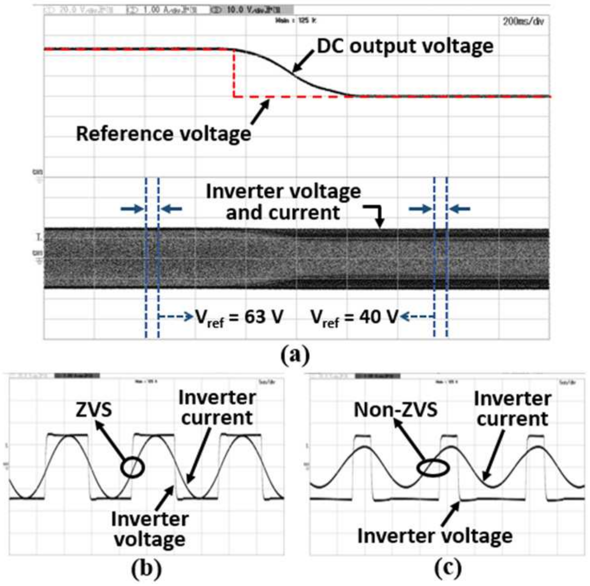

Fig.17: *(a) Experimental results of non-ZVS operation due to output voltage control with fixed frequency (Step decrease in output voltage reference from 63 to 40 V). (b) Enlarged view of inverter voltage and current under* $V_{ref} = 63$ *V. (c) Enlarged view of inverter voltage and current under* $V_{ref} = 40$ *V.*

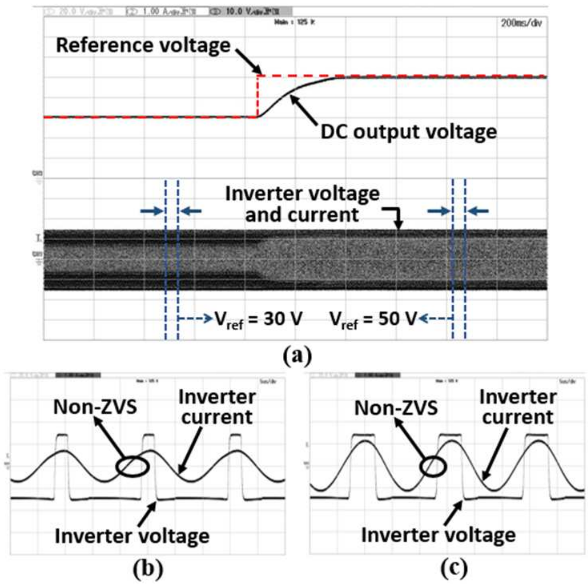

Fig.19: *(a) Experimental results of non-ZVS operation due to output voltage control with fixed frequency (Step increase in output voltage reference from 30 to 50 V). (b) Enlarged view of inverter voltage and current under* $V_{ref} = 30$ *V. (c) Enlarged view of inverter voltage and current under* $V_{ref} = 50$ *V.*

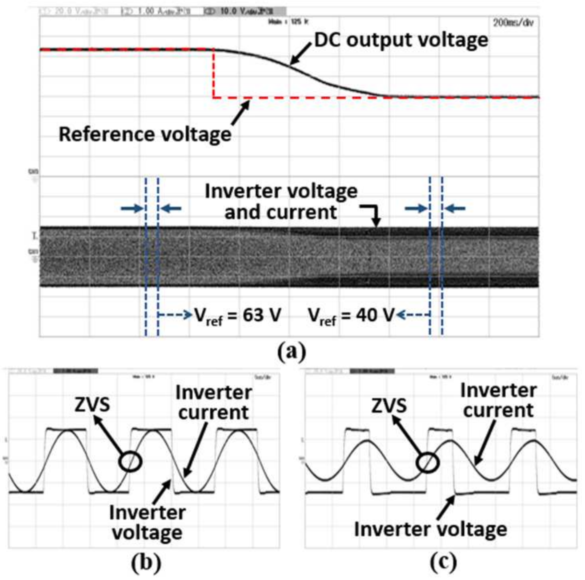

Fig.18: *(a) Experimental results of ZVS operation due to output voltage control with variable frequency (Step decrease in output voltage reference from 63 to 40 V). (b) Enlarged view of inverter voltage and current under* $V_{ref} = 63$ *V. (c) Enlarged view of inverter voltage and current under* $V_{ref} = 40$ *V.*

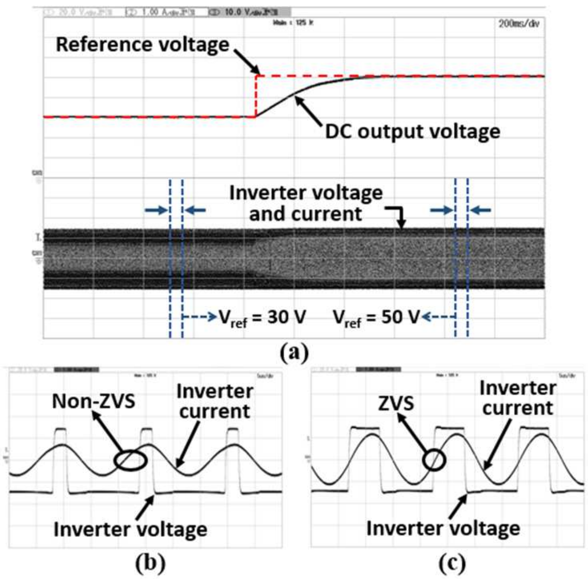

Fig.20: *(a) Experimental results of ZVS operation due to output voltage control with variable frequency (Step increase in output voltage reference from 30 to 50 V). (b) Enlarged view of inverter voltage and current under* $V_{ref} = 30$ *V. (c) Enlarged view of inverter voltage and current under* $V_{ref} = 50$ *V.*

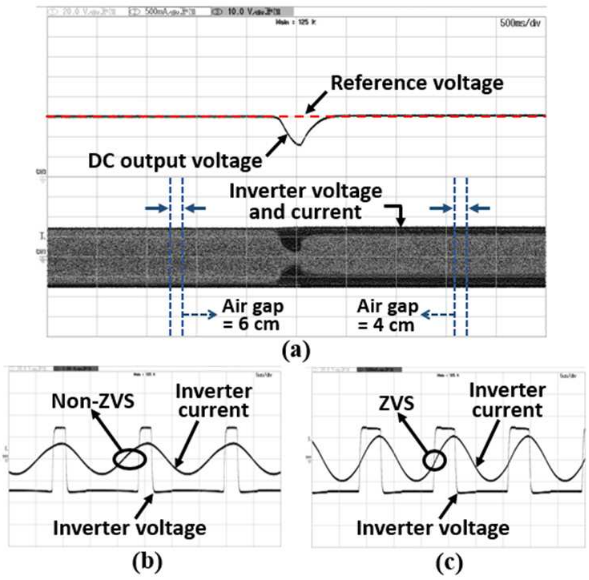

Fig.21: *(a) Experimental results of ZVS operation due to output voltage regulation with variable frequency (Step decrease in air gap from 6 to 4 cm). (b) Enlarged view of inverter voltage and current under Air gap = 6 cm. (c) Enlarged view of inverter voltage and current under Air gap = 4 cm.*

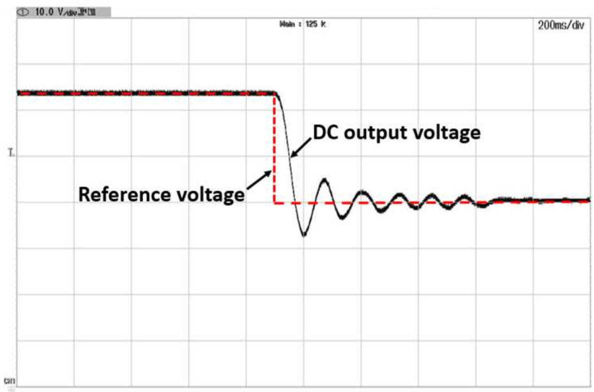

Fig.22: *Experimental results of output voltage response with changing step of duty cycle in the microcontroller.*

switching frequency, as seen in Fig. 20 (c).

The change in the air gap caused the magnetic coupling (k) to change which resulted in output voltage variation. However, with the proposed controller, the output voltage can be regulated. For example, if the air gap is decreased then, the coupling coefficient k is increased. This causes the output voltage to be reduced. From the flowchart in Fig. 15, the duty cycle must be increased to adjust the output voltage while keeping the system operating in a ZVS mode through switching frequency variation. The experimental results of DC output voltage regulation for the case of a changed air gap distance is shown in Fig. 21. The reference voltage is set to 30 V. The coefficient, k, was increased from 0.38 to 0.52 by decreasing the air gap from 6 cm to 4 cm. This caused the output voltage initially decreased. Then, it was restored to 30 V with ZVS operation by automatically increasing the duty cycle and switching frequency. Thus, from the results shown in Figs. 17–21, the proposed controller can be validated.

Fig. 22 shows the output voltage response when the duty cycle step was increased from 0.02 to 0.2. The output voltage response had a higher overshoot and longer settling time compared with the results in Fig. 18. This was due to an inappropriate duty cycle change step. As stated earlier, an empirical method was used to select the changing step for simplicity. An optimal controller design and system stability analysis will be done in future work.

An efficiency comparison of the ADC control with fixed and variable frequency for the same angle and output power is shown in Fig. 23. The efficiency of a variable frequency control was higher than for fixed frequency control at all α angles due to a lower power-up switching loss. With $\alpha = 0°$, both controls had the same efficiency of 74.3%. Once the output power was decreased, indicated by an increase in the α angle, the difference became obvious. At $\alpha = 135°$, the efficiency of the proposed variable frequency control was 13.7% higher.

6. CONCLUSIONS

The output voltage control of the SP topology IPT system using a primary side controller is proposed in this paper. The absence of a DC-DC converter and secondary side controller reduces the cost, size and complexity of the system. An ADC control method was implemented on a full-bridge inverter to control the DC output voltage through the inverter voltage. In addition to ZVS operation, the switching frequency of the inverter circuit was also varied. Theoretical analysis of the non-ZVS mode due to load and α angle variations was performed based on a mutual inductance coupling model.

Simulation and experimental studies were performed. Experimental results of the DC output voltage control due to reference voltage and magnetic coupling variations validated the proposed controller. The system efficiency was improved and this become obvious as the output power was reduced. An optimal controller design and system stability analysis will be done in our future work.

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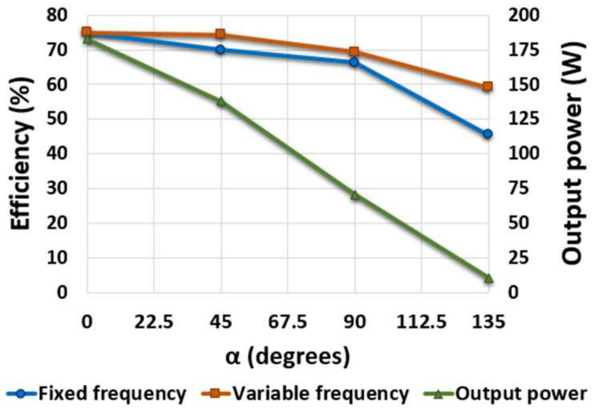

Fig.23: *Experimental results of the efficiency comparison between fixed and variable frequency control.*

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