ZVS-Operation of LLC Resonant Inverter with Phase Limit Control for Induction furnace

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ABSTRACT

This paper presents an LLC resonant inverter with phase limit control to guarantee zero voltage switching (ZVS) operation and protect switching devices from spike current during the heating process. The output power is controlled by using the asymmetrical duty cycle (ADC) modulation. With phase limit control, the non-ZVS operation and spike current caused by a change of duty cycle with fixed frequency and load Curie's temperature can be eliminated. The proposed method is confirmed through computer simulation and hardware experiment. The experimental results are provided with the heating of a 300 g of Tin from room temperature until melting at 232 °C.

Keywords: LLC Resonant Inverter, Induction Furnace, Asymmetrical Duty Cycle, Phase Limit

1. INTRODUCTION

Induction heating (IH) technology has become more importance role in recent year because of its cleanliness, safety for user, fast heating and controllable. Moreover, IH technology is used in many applications such as melting, welding, hardening and cooking. IH applications use a high current passing through an induction coil to produce sufficient magnetic field and Eddy current within work pieces. The operating frequency is selected by the heating application [1]. A resonant circuit is commonly used in the IH application to produce the high current and high voltage to produce maximum output power to the heating load. Recently, the LLC resonant topology has been introduced which has many advantages such as high current gain, short circuit immunity and lower current on the secondary side of a transformer [2].

The IH appliances are designed to operate with high efficiency, wide control range, compactness and reliability. However, main research efforts have been focused on power control strategy. For example, the asymmetrical voltage cancellation (AVC) is used to control the output power by varying the duty cycle with fixed or variable frequency [3]-[5]. The pulse frequency modulation (PFM) is proposed in output power control by adjusting the switching frequency [6]. Similarly, an algorithm like the phase shift modulation (PS) is also used in output power control by shifting the phase difference between the two upper switches [7]. For the asymmetrical duty cycle (ADC) technique, the output power can also be controlled by varying the duty cycle [8]. Although, the PFM is commonly used in IH applications due to its simplicity but it may introduce a problem in melting applications due to a requirement of high skin depth. This means that the inverter must be operated in the range of low to medium frequency to maintain the required skin depth of the work piece. Therefore, a power control by using the PFM technique with a low quality factor load may need to operate at high frequency when the output power is reduced by increasing the switching frequency and the switching loss will be increased. For a high quality factor load, it is difficult to control the output power with the PFM technique because of its narrow bandwidth characteristics. In contrast, the output power control by using ADC control technique can be implemented with both high and low quality factor loads, with no sacrifice on the range of power and simplicity of gating signal circuits.

It is widely known that the switching devices can be damaged from a non-ZVS operation and spike current during the duty cycle adjustment with fixed frequency to vary the output power and when the load parameter is changed due to the work-piece temperature is close to the Curie's temperature. Therefore, the switching frequency must be controlled when the duty cycle and load parameters are varied to maintain the ZVS operation and prevent the switching device from the spike current. This paper proposes an asymmetrical duty cycle control with phase limit technique to guarantee the ZVS operation and protect the switch from spike current during the heating process. The phase difference between the voltage and current of the switching device is limited to a minimum value where the ZVS operation can be obtained by varying the switching frequency. With the proposed method, the skin depth control is more accurate compared with the PFM control. This feature is rather essential in melting applications. The val-

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idation of the proposed controller is set up by the experiment of melting a 300 g of Tin from room temperature to melting point at 232 °C.

The paper is organized as follows. Section 2 presents analysis of the asymmetrical duty cycle control technique. Section 3 shows analysis of the ZVS operation with ADC control technique. Section 4 explains the proposed control strategy to keep the ZVS operation. Section 5 shows a design example of major component. Section 6 shows the simulation and experimental results. The conclusion of this paper is shown in Section 7.

2. FULL-BRIDGE LLC RESONANT INVERTER

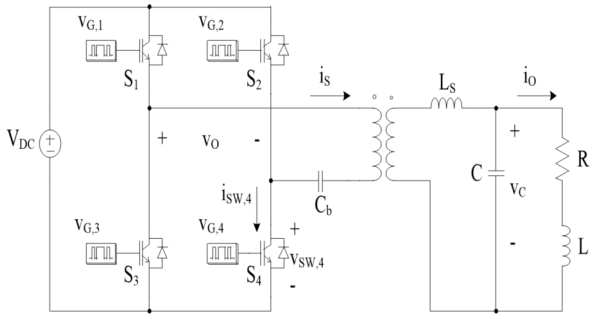

Fig.1: *Full-bridge LLC resonant inverter.*

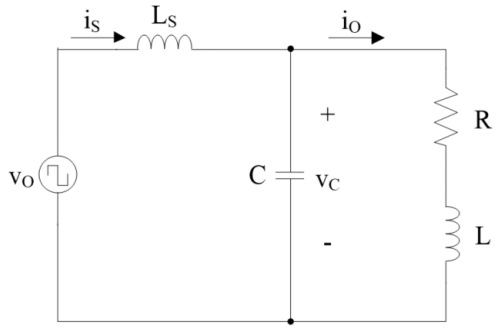

Fig.2: *Equivalent circuit.*

2.1 Circuit Description

The full-bridge LLC resonant inverter under study is shown in Fig. 1. It consists of four IGBT switches with anti-parallel diode (S_1-S_4), a matching transformer, a dc blocking capacitor (C_b), a series inductor (L_s), a resonant capacitor (C), an equivalent resistor (R) and inductor (L) of the heating coil. A simplified equivalent circuit of Fig. 1 can be illustrated in Fig. 2 and a dc blocking capacitor can be neglected. Therefore, the voltage source can be seen as an asymmetrical ac voltage supplied to the load.

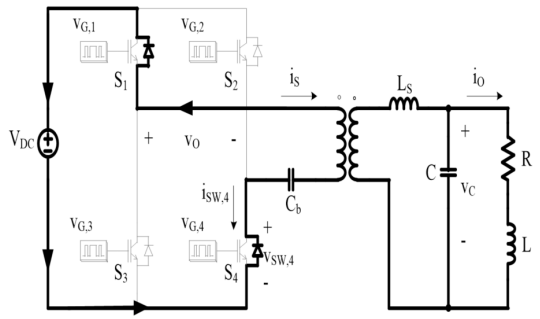

Fig.3: *The inverter operation at mode 1 (t_0-t_1).*

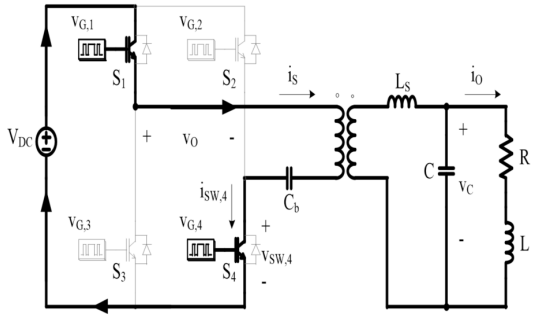

Fig.4: *The inverter operation at mode 2 (t_1-t_2).*

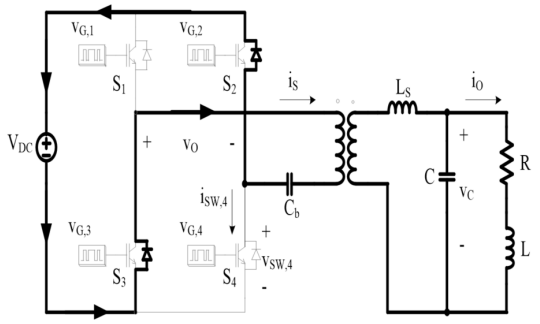

Fig.5: *The inverter operation at mode 3 (t_2-t_3).*

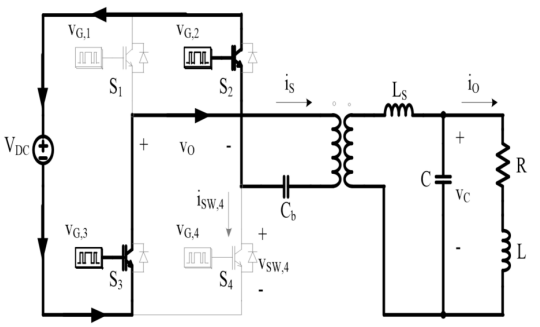

Fig.6: *The inverter operation at mode 4 (t_3-t_4).*

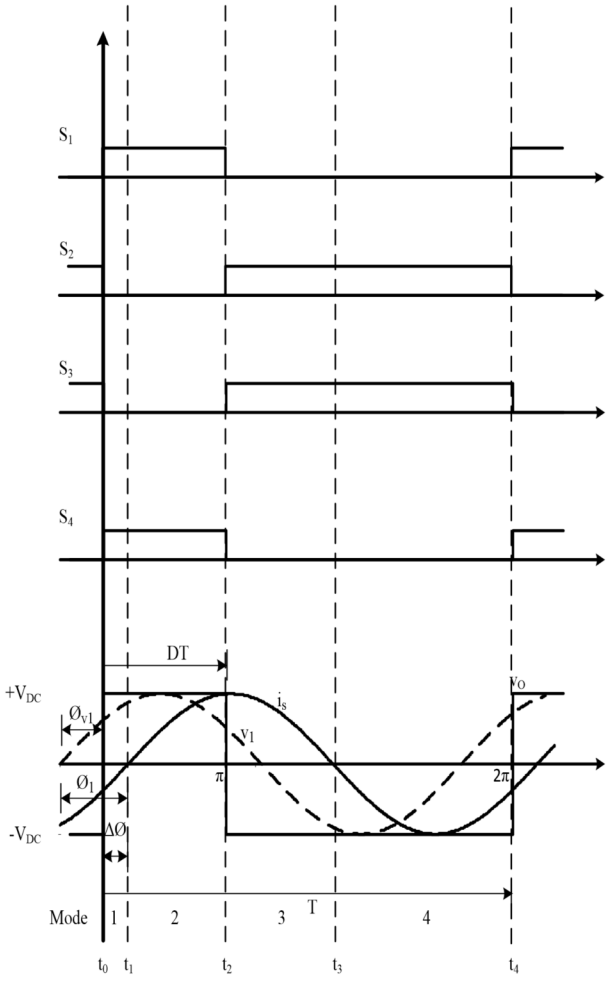

Fig.7: *The output voltage and current waveform of the inverter.*

2.2 Modes of Operation

The inverter has been designed to operate beyond the resonant frequency to keep the ZVS operation. Thus, the inverter has four operation modes as illustrated in Fig. 7. Modes of operation are shown in Figs. 3-6 where D and T are duty cycle and period of the gate signals, respectively.

and explained as follows.

1) Mode 1 (t_0-t_1): While switches S_1 and S_4 are turned on and switches S_2 and S_3 are turned off at t=t_0, the negative current input i_S flows through diodes D_1 and D_4 to the load.
2) Mode 2 (t_1-t_2): At t=t_1, anti-apparel diodes D_1 and D_4 are turned off. The positive input current i_S flows through switches S_1 and S_4.
3) Mode 3 (t_2-t_3): While switches S_1 and S_4 are turned off, both switches S_2 and S_3 receive positive gating signals at t=t_2. Diodes D_2 and D_3 conduct by the positive current input i_S similar to that in Mode 1.
4) Mode 4 (t_3-t_4): At t=t_3, anti-apparel diodes D_2 and D_3 are turned off. The negative current input i_S flows through switches S_2 and S_3.

2.3 Analysis of Output Power

The switching frequency of the inverter is designed to operate beyond the resonant frequency which can be calculated by [4].

$$\omega_0 = \sqrt{\frac{L + L_S}{L \cdot L_S \cdot C}} \tag{1}$$

From Fig. 2 the impedance as seen by the output voltage (V_O) can be expressed by [2]

$$Z_{Total}(j\omega_0) = \frac{R\omega_0 {L_S}^2 \left(\omega_0 L^2 + jR(L_S + L)\right)}{\omega_0^2 L^4 + R^2 \left(L_S^2 + 2L_S L + L^2\right)} \tag{2}$$

At the resonant frequency, the LLC load configuration is not equal to resistive load as shown in (2) and the switching angle (ϕ_1) can be calculated by

$$\phi_1 = \tan^{-1} \frac{R(L_S + L)}{\omega_0 L^2} \tag{3}$$

and series inductance can be expressed as

$$L_S = \frac{L^2 \omega_0}{R} \tan\phi - L \tag{4}$$

The current gain at resonance can be calculated by [4]

$$\frac{I_O}{I_S} = \frac{I_S}{L} \cos\phi \tag{5}$$

The relationship between the output voltage of the inverter (V_O) and the load voltage (V_C) can be calculated as

$$V_C = \frac{R + j\omega L}{(j\omega L_S \times j\omega C)(R + j\omega L) + j\omega L_S + R + j\omega L} \times V_O \tag{6}$$

For the first harmonic approximation of V_O, the load voltage (V_C) can be simplified as

$$V_C = \left(-\frac{L}{L_S} - j\frac{L^2}{RL_S}\sqrt{\frac{L + L_S}{L \cdot L_S \cdot C}}\right) \times V_1 \tag{7}$$

where V_1 is the fundamental voltage of V_O in see Fig. 7 which has the Fourier series coefficient as

$$\hat{V}_1 = \frac{2V_{DC}}{\pi}\sqrt{a_n^2 + b_n^2} \tag{8}$$

$$\phi_{vn} = \tan^{-1}\left(\frac{a_n}{b_n}\right) \tag{9}$$

$$a_n = \sin(2n\pi D) \tag{10}$$

$$b_n = 1 - \cos(2n\pi D) \tag{11}$$

where V_{DC} is dc input voltage, ϕ_{vn} is the phase angle of nth harmonic and D is the duty cycle of V_O. Therefore, the amplitude of V_1 and ϕ_{v1} can be calculated as,

$$\hat{V_1} = \frac{4V_{DC}}{\pi}\sin(\pi D) \tag{12}$$

$$\phi_{v1} = \tan^{-1}(\cot(\pi D)) \tag{13}$$

The average power at the load is given by

$$P = V_1^2 \mathrm{Re}\left\{Z_{Total}(j\omega_0)^{-1}\right\} \tag{14}$$

Thus,

$$P = \frac{2{V_{DC}}^2}{R\pi^2}\left[\sin^2(2\pi D) + (1-\cos(2\pi D))^2\right] \times \left(\frac{L}{L_S}\right)^2 \tag{15}$$

The relationship in (15) shows that the average power at the load is dependent on the duty cycle. So, the output power can be controlled by varying the duty cycle of the gate signal.

3. ZERO VOLTAGE SWITCHING ANALYSIS

The inverter has been designed to operate near the resonant frequency to keep the ZVS operation mode. Thus, the output current (i_s) can be assumed to be a sinusoidal waveform and expressed by

$$i_s(t) = \hat{I}_S \sin(\omega t - \Delta\phi) \tag{16}$$

And the phase angel of the current is $\Delta\phi$ is given as,

$$\Delta\phi = \phi_1 + \phi_{v1} \tag{17}$$

Since, the phase angle of the fundamental voltage (ϕ_{v1}) in (13) increases when the duty cycle D is decreased as shown in Fig. 8, this results in that the phase angle $\Delta\phi$ becomes negative. From (15), the maximum power is obtained at 50% duty cycle. This is the point where the highest efficiency is observed. If the duty cycle is varied, the output power and efficiency are decreased, regardless of the direction of change. Since the proposed method is based on the ADC switching scheme, the limit of 50% is imposed on the duty cycle. As demonstrated in Fig. 7, the current is leads the voltage v_o and the inverter is operated in non-ZVS operation.

4. PROPOSED CONTROL STRATEGY

To avoid the mentioned non-ZVS operation, the switching frequency has effected on the inductive load. This will cause the phase current $\Delta\phi$ of the current is to increase and the inverter regains the ZVS operation. The non-ZVS condition in the ADC technique is addressed by proposing a phase limit to avoid

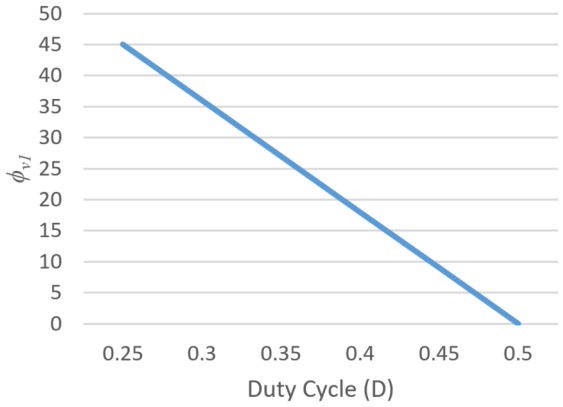

Fig.8: *The relationship between phase angle of fundamental voltage of the inverter and duty cycle.*

negative phase angle by increasing the switching frequency while varying the duty cycle to control the output power.

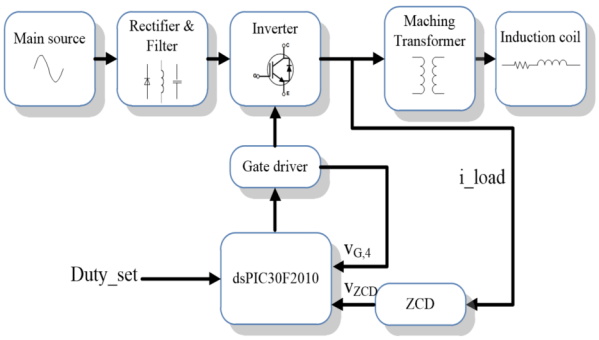

Fig.9: *Block diagram of an induction furnace system.*

The proposed induction furnace system is shown in Fig. 9 where the inductance of heating coil are dependent on the geometry, conductivity, relative permeability and temperature. When the temperature of the work piece is close to the Curie's temperature, the relative permeability is decreased. This in turn affects to the equivalent inductance of the work piece. Hence, the resonant frequency is changed during the heating process. Moreover, the duty cycle variation of the ADC control with fixed frequency will cause a spike current under non-ZVS operation. Thus, the controller must be able to adjust the switching frequency to keep the ZVS operation and protect the switching device from the spike current.

The control part as shown in Fig. 9 consists of a dsPIC microcontroller, gate driver circuits, a current sensor, a zero crossing detection (ZCD) circuit. The control principle is illustrated in Fig. 10. The "Duty_set" is a duty cycle required to adjust the output power which can be obtained by the push button switch outside of the controller and "Phase" is a phase difference between the voltage and current of

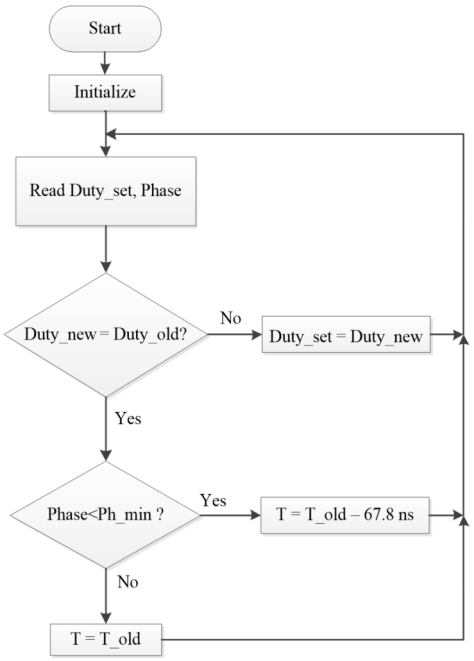

Fig.10: *Flowchart of a controller.*

the inverter. The ZCD circuit is used to detect the phase of the current and sends the output signal to the dsPIC microcontroller. If "Phase" is less than a minimum value (Ph_min), the controller will increase the switching frequency by reducing the switching period of 2 machine cycles (67.8 ns). The output signal of the controller is a gate signal with various duty cycle and frequencies to a full-bridge inverter.

5. DESIGN PROCEDURE

With the proposed control described in the previous section in mind, a design example of major components in Fig.1 are provided as follows.

5.1 Resonant Load

The resonant load consists of a series inductor, resonant capacitor, heating coil and 300 g of Tin as a workpiece in the crucible. The desired operating frequency is at 35 kHz. The heating coil has an equivalent resistance and equivalent inductance of 61.2186 mΩ and 7.39016
muH, respectively. The targeted application is a 600 W induction furnace for a 300 g Tin workpiece. The switching angle is set to 18° and the series inductor is obtained using (4) as,

$$L_S = \frac{L^2\omega_0}{R}\tan\phi - L = 58.18 \approx 59\mu H$$

The resonant capacitor is obtained from (1) as

$$C = \frac{L + L_S}{{\omega_0}^2 \cdot L \cdot L_S} = 2.98\mu F$$

Due to availability, two of 1 kV, 1.5 μF capacitors are used as resonant capacitors and the resonant frequency is slightly modified to

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{L + L_S}{L \cdot L_s \cdot C}} = 38.86 \text{ kHz}$$

From (5), the current gain can be calculated as

$$\frac{L_S}{L}\cos\phi = 7.6$$

5.2 Matching Transformer

The current gain as calculated from (5) is not sufficient to heat a 300 g Tin workpiece from room temperature to the melting point at 232 °C. Thus, a matching transformer is introduced and the current input $I_{S,rms}$ is found from

$$I_{S,rms} = \frac{\pi P}{2\sqrt{2}V_m\cos\phi} = 2.25\text{A}$$

The full-load current of 99 A is used to heat a 300 g Tin workpiece to the desired temperature. Thus, the transformer ratio can be found from

$$n = \frac{I_{full-load}}{\frac{L_S}{L}\cos\phi \times I_{S,rms}} = 5.76 \approx 6$$

6. SIMULATION AND EXPERIMENTAL RESULTS

6.1 Simulation Analysis

To analyse the proposed control strategy, the computer simulation of the system with the parameters shown in Table 1 have been investigated. The voltage and current of the switching device when operating at 50% and 40% duty cycle with fixed frequency are compared. The ZVS operation can be achieved with 50% duty cycle which increases the efficiency and reduces the stress on the switching devices. When the duty cycle is changed to 40%, the non-ZVS operation is occurred as shown in Fig. 11. This can damage the switching devices and increase switching loss. To achieve the ZVS operation, the switching frequency must be increased when duty cycle is changed as shown in Fig. 12. The voltage and current waveforms of the inverter and load when operating at 50% duty cycle is shown in Fig. 13. The case of 40% duty cycle is shown in Fig. 14.

6.2 Experimental Results

To validate the proposed control, a hardware prototype of induction melting is created as shown in Fig. 15. It consists of a graphite crucible of 60 mm in diameter and 85 mm in high with a 300 g of Tin as a work-piece inside a crucible. The heating is performed from room temperature until the work piece

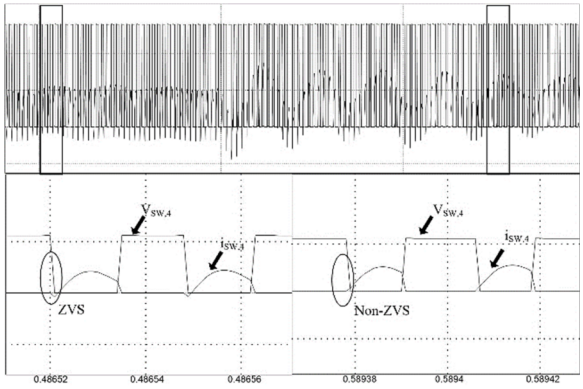

Fig.11: *The transient response at a switch S4 while reduce the duty cycle from 50% to 40% with fixed frequency.*

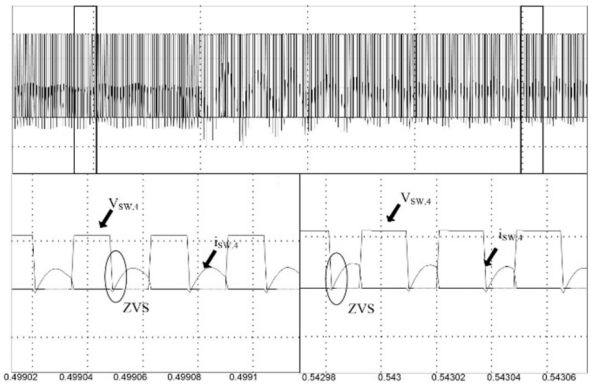

Fig.12: *The transient response at a switch S4 while reduce the duty cycle from 50% to 40% with variable frequency.*

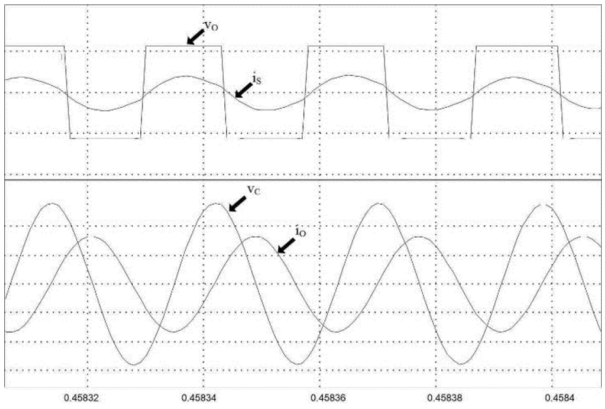

Fig.13: *v_O, i_S, v_C and i_O waveforms at 50% duty cycle.*

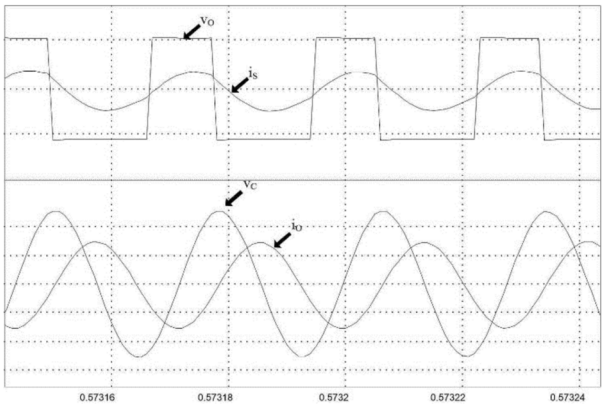

Fig.14: *v_O, i_S, v_C and i_O waveforms at 40% duty cycle.*

Table 1: *System Parameters.*

Transformer ratio, $n = n_1/n_2$	6
Equivalent Resistor, R	61.2186 mΩ
Series inductor, L_S	59 μH
Induction coil inductor, L	7.39016 μH
Resonant capacitor, C	3 μF
Switching frequency, f_s	35.70 - 38.10 kHz
DC blocking capacitor, C_b	1.5 μF
Input Voltage, v_{AC}	220 V_{rms} , 50 Hz
DC Bus Voltage, v_{DC}	311 V

is melted at 232°C. The switching frequency is automatically controlled from 35.70 to 36.10 kHz to limit the phase difference of the switch's voltage and current. The duty cycle is varied from 10% to 50% to control the output power.

The input and output signals of the ZCD circuit is shown in Fig. 16 where the phase difference can be obtained by comparing the rising edge of the gate signal ($v_{G,4}$) with the output of the ZCD circuit (v_{ZCD}) using the input capture function of the controller. As shown in the transient response in Fig. 17, the spike current occurs at a switch when reducing the duty cycle from 50% to 40% under fixed frequency. With the proposed phase limit control, the ZVS operation is achieved as mentioned by automatically increasing the switching frequency when the duty cycle is changing from 50% to 40%, as shown in Fig. 18. The experimental waveforms of the voltage and current from the inverter and load when the duty cycle is at 50% and 40% are shown in Figs. 19 and 20, respectively. The inverter efficiency is in the range of 80% to 90 %, as shown in Fig. 21. With the control of switching frequency, the highest efficiency reaches 90% at 50% duty cycle. At this point, the LLC topology has a better performance for high quality factor load and the minimum switching angle is not over 20°

($\phi_1 < 20°$).

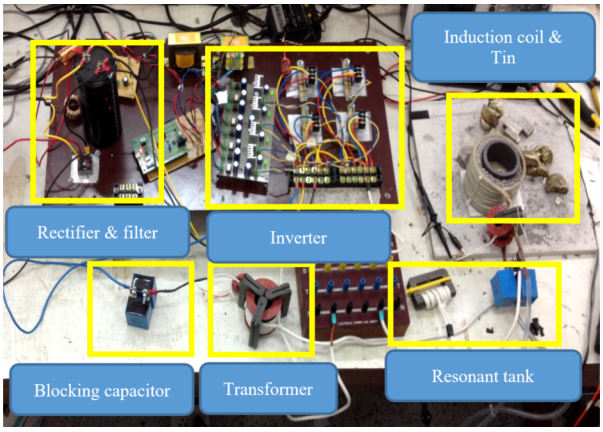

Fig.15: *The hardware prototype.*

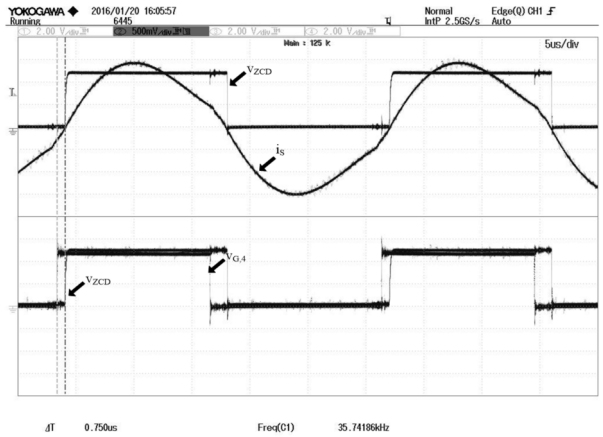

Fig.16: v_{ZCD}, i_S *and* $v_{G,4}$ *waveforms.*

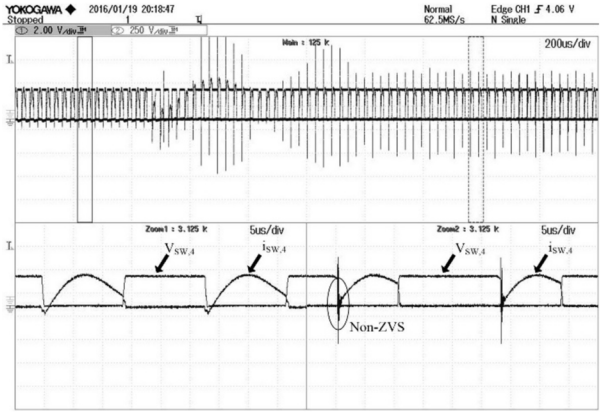

Fig.17: *The transient response at a switch S4 while reduce the duty cycle from 50% to 40% with fixed frequency.*

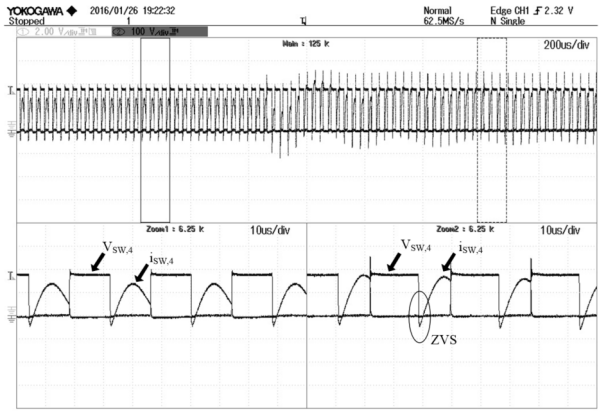

Fig.18: *The transient response at a switch S4 while reduce the duty cycle from 50% to 40% with variable frequency.*

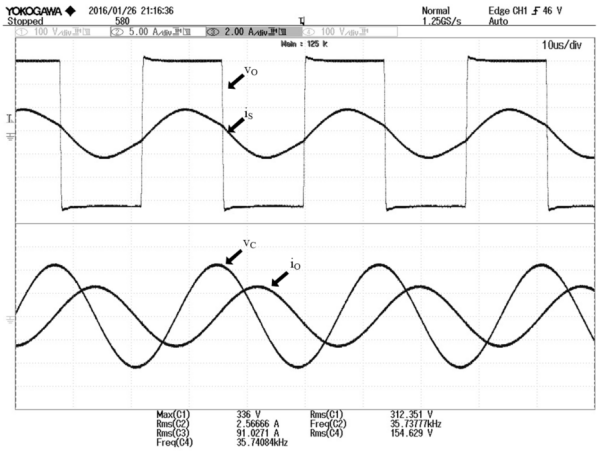

Fig.19: v_O, i_S, v_C *and* i_O *waveforms at 50% duty cycle.*

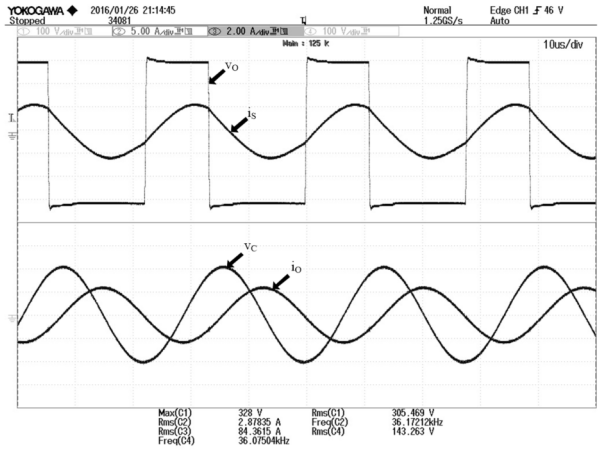

Fig.20: v_O, i_S, v_C *and* i_O *waveforms at 40% duty cycle.*

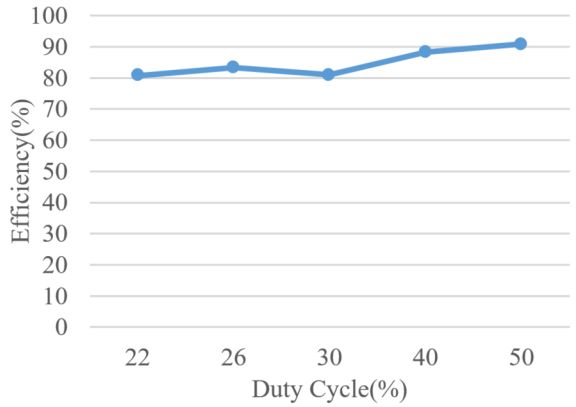

Fig.21: *The inverter efficiency.*

7. CONCLUSION

A power control of an LLC resonant inverter for induction furnace using the ADC technique with phase limit control to guarantee the ZVS operation during the heating process has been proposed in this paper. The output power is controlled by adjusting the duty cycle of the gate signal and the problem with the non-ZVS operation and spike current when changing the duty cycle with fixed frequency and load parameter variation can be eliminated by an automatic increase of the switching frequency with the aim for a phase difference greater than the minimum phase limit. Simulation and experimental results of an induction melting of a 300 g Tin work piece from room temperature to the melting point at 232°C have been presented to validate the proposed control method.

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