RGB LED Driver Circuit Design For An Optical Fiber Sensor System

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ABSTRACT

In this paper, the design of a programmable mixed-signal electronic circuit to control the light output of a red-green-blue (RGB) light emitting diode (LED) to be used in an optical fiber sensor system is presented and discussed. The LED is to be used as a light transmitter (light source) within the sensor system. The output of each LED color is to be independently controlled using either a d.c. current or a pulse width modulation (PWM) encoded current. The idea for, and architecture of, the mixed-signal electronic circuit design is considered as both a discrete implementation using off-the-shelf components and the concept for an application specific integrated circuit (ASIC) solution using a 0.35 μm complementary metal oxide semiconductor (CMOS) fabrication process. In this paper, the design operation principles, circuit architecture, simulation results and hardware requirements for this LED driver circuit are considered.

Keywords: Optical Fiber Sensors, Light Emitting Diode, Programmable Logic Device, Mixed-Signal Integrated Circuit Design, Simulation

1. INTRODUCTION

In everyday life, sensors are required to measure physical quantities allowing for an indication of the status of a medium being sensed. A range of analog and digital sensors can be deployed along with a variation in the design and operation of the electronic circuit hardware (and if appropriate, software) used. The choice of sensor and design of the electronic system would be based on the requirements of the specific application considered.

In recent years, sensors based on the transmission of light with a known characteristic through a medium to be sensed, and detecting the characteristics of the resulting light received have been developed [1, 2]. The light will be modulated as it passes through the medium and the differences between the transmitted and received light will indicate the characteristics of the medium being sensed. ***Fig. 1*** shows the type of optical fiber sensor system considered in this work. The electronics (the parts within the dashed box area) provide the necessary electrical signals, which are applied to the sensor and medium to be sensed via an electrical-optical transducer (the light transmitter) and an optical fiber cable link. The response in the form of an optical signal is converted back to an electrical signal by the light receiver (optical-electrical transducer). Hence, the sensor and medium are optically rather than electrically connected to the electronics. The signals are then processed, usually by a software programmed processor or via a hardware configured programmable logic device (PLD). For correct operation, the power supply and external communications sub-systems are also required. This paper considers the design of a LED driver circuit for use in optical fiber sensor systems. Specifically, the design and analysis of a RGB (e.g., [3]) LED driver operating on a single +3.3 V power supply for use in the sensor light source are presented.

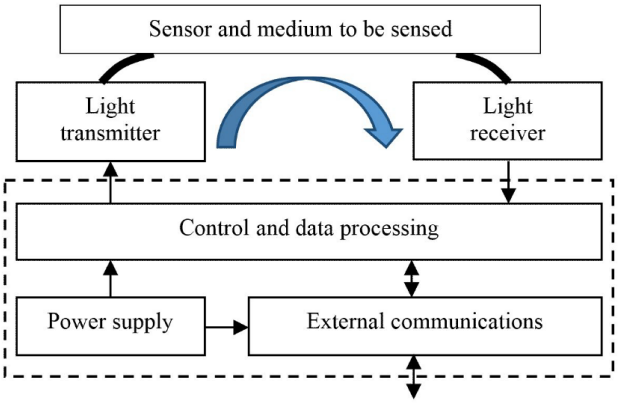

Fig.1: *Optical fiber sensor system overview.*

The LED is considered here as it is a physically small and low-cost light source that can be readily controlled using analog or digital circuit techniques. In prior work, where the LED has been considered as a suitable light source for an optical fiber sensor system, a single color has been used [4]. It is typical in such systems to use a red color LED with a wavelength of about 650 nm. In this work, the single color LED concept is extended to three colors (red, green

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and blue (RGB)) using a single RGB LED. Each color can be independently controlled by varying the LED current and this can be achieved via a processor with software coding (e.g., using a microcontroller (μC)) or in digital logic using a PLD (CPLD (complex programmable logic device) or FPGA (field programmable gate array)). Therefore, it can produce a programmable intensity light source that extends the capabilities of a single color LED arrangement within an optical fiber sensor system design. Given the ability to control the intensity of light from three light sources, the effect of combining sensor results from combinations of wavelength (e.g., red light only, red with green) may be used with different sensors in order to improve sensor operation. In addition, the work considers the use of the PLD to implement the required digital sub-system functions in custom hardware rather than the common approach of processor based software coding. Such a PLD based approach can extend the ability of the system to embed high-speed and parallel digital signal processing (DSP) for local sensor data processing. The main discussion within the paper considers the design, prototyping and evaluation of a discrete prototype system.

The paper is structured as follows. Section 2 will discuss the main characteristics of an optical fiber sensor system with a focus on the electronic circuit aspects. Based on this discussion, the light transmitter part of the sensor system is presented with a focus on using an RGB LED as the light source. Each color would be uniquely controllable, hence a range of light source colors would be possible. Section 3 will present the architecture and principle of operation of the programmable RGB LED driver circuit design. Section 4 will present a set of simulation results for the analog part of the design and specific prototype test results, considering both the digital logic output and analog circuit operation. Section 5 will consider the requirements for a CMOS ASIC version of the design. Section 6 will conclude the paper.

2. OPTICAL FIBER SENSORS

2.1 Introduction

An optical fiber (fibre) sensor [5, 6] is a type of sensor that uses an optical fiber cable either as the sensing element or as a means of connecting a remote sensor to the electronic circuit that provides a sensor stimulus input and processes the sensor output signals. The electronic circuit produces an electrical signal (the stimulus) and converts this electrical signal to an optical signal to apply to the sensor. The optical signal is then propagated through the fiber and sensor. Once the light signal has been modified by the medium being sensed, the result is received by the same or a different electronic circuit that converts the light signal back into an electrical signal for analysis and communication to an external system. Optical fibers can be used as sensors to measure physical quantities such as:

- Stress and strain
- Temperature
- Pressure
- Pollution

The quantity to be measured modifies the light signal as it passes through the sensor and, as the sensor does not use electrical signals, it can be used in certain applications where electrical signals could be problematic such as:

- Environments subject to electromagnetic interference
- High voltage signal levels
- Applications involving flammable materials where the potential for an electrical fault could a cause a fire

The operating principles of the optical fiber sensor are shown in ***Fig. 2.*** Two types of sensor arrangement are identified:

1. In the top image (a), an extrinsic optical fiber sensor is shown. In this arrangement, the light from light source is transmitted to the sensor and the response is returned along the optical fiber cable to the light detector. Sensing occurs in a region outside the sensor and the fiber acts to pass light from the light source to the detector.
2. In the bottom image (b), an intrinsic optical fiber sensor is shown. In this arrangement, light from the light source is transmitted to the sensor and the response is returned along the fiber to the light detector as before. However, with the intrinsic optical fiber sensor, the physical properties of the fiber undergo a change that is due to a physical phenomenon, e.g., stress that mechanically alters the fiber. The fiber itself acts as the sensor.

Hence, the optical fiber can be used to either transmit light only or to both transmit light and act as the sensor. Note, however, that the choice of the fiber material is important. Both glass optical fiber (GOF) and plastic optical fiber (POF) cables are widely used, depending on the requirements of the system. Recently, POF has gained interest for use in sensor systems given its lower cost, greater flexibility and resilience to mechanical bending, shock and vibration [7].

2.2 Light source, optical fiber and detector

The light source is required to convert an electrical signal into an optical signal and provide a light output of a known characteristic.

The choice of light source depends on a number of requirements, with the light signal wavelength and intensity being of primary concern. A white light source would emit visible white light with a broad optical bandwidth. This can be used in a system to detect the amount of absorbed light at particular

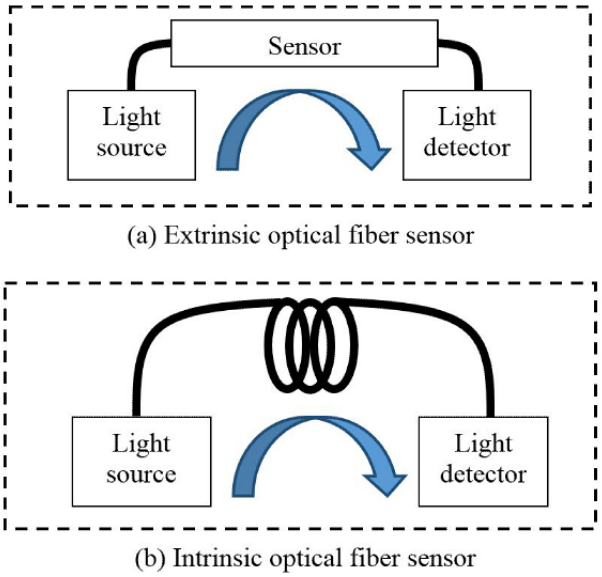

Fig.2: *Optical fiber based sensing.*

wavelengths within the optical bandwidth. Hence, the effect of the medium on particular wavelengths of light would be of interest. Other light sources would emit a single wavelength, or a narrow optical bandwidth, and hence the effect of the medium on the amount of light absorbed by the medium at the selected light source wavelength would be of interest. In this second type of light source, the choice of device to use would either be a semiconductor laser or a semiconductor LED. Typically, though not exclusively in sensor systems, red light with a wavelength range of approximately 630 nm to 700 nm is used [8, 9]. The laser would provide for a coherent light source with the potential for high data rates and transmission over long distances. The LED would provide for a non-coherent light source with lower data rates and shorter transmission distances when compared with the semiconductor laser. However, a major advantage of the LED is its lower cost and, therefore, advantageous in cost sensitive applications. In optical fiber sensor systems, the advantages of high data rates and transmission over long distances are not major factors in the choice of the light transmitter as the optical fiber cable lengths used are relatively short and high speed digital data transmission is not a major requirement for correct system operation.

The optical fiber provides the means to transmit the light to the medium and to receive the light passed through the medium at the light detector. In some sensors, the fiber also acts as the sensor.

The light detector is required to convert the optical signal back into an electrical signal. In white light source systems, the detector must be capable of detecting light over a broad optical bandwidth. Typically, this is achieved using a spectrometer. The spectrometer separates the light into its spectral components that are then captured and the intensity of the light at different wavelengths is provided. In systems where a single wavelength or a narrow optical bandwidth light source is used, the light detector would be a semiconductor photodiode or phototransistor. These devices produce a current output that is typically converted to a voltage and sampled using an analog-to-digital converter (ADC) of suitable speed and resolution. Once digitized, the signal can then be processed using suitable DSP techniques. The advantage of the spectrometer is in the detail of information provided in the optical bandwidth that the spectrometer is designed to work over. However, the spectrometer is a physically large and expensive instrument. The photodiode and phototransistor have the advantage of lower cost, but with a trade-off in information detail as they would be sensitive to a narrow band of wavelengths only.

3. RGB LED DRIVER CIRCUIT

3.1 Introduction

In some optical fiber sensor systems, the LED is used as the light source [10, 11]. The LED is a semiconductor device that converts an electrical signal into an optical signal. The properties of the semiconductor material cause photons of a specific wavelength to be emitted and an electronic circuit is used to control the emission of light. The flow of electrical current hence causes light to be emitted and:

1. The wavelength of the light emitted is dependent on the semiconductor material
2. The intensity of the light emitted is dependent on the value of the electrical current

In the work described here, the system considers the use of an RGB LED as the light transmitter and a POF as the light transmission medium and potentially the sensor. Only the light transmitter circuit is considered in this paper. The choice of the RGB LED is based on two considerations. Firstly, light of different wavelengths (red light at about 650 nm, green light at about 510 nm and blue light at about 475 nm) may respond differently within the medium, such as the amount of light absorbed by the medium. Hence, the use of multiple color combinations may provide additional information. Secondly, if one color is not absorbed by the medium, it may be used as an optical reference for a second color that would be absorbed by the medium. The focus is on developing an easy to use, flexible and programmable RGB LED driver circuit that can be used as a plug-in module to be inserted into a range of possible sensor systems. The module is communicated to via a software programmed processor or programmable logic device. The LED driver circuit would be programmable via current sensing resistors and digital codes from the connected digital electronics. The value of the current sensing resistor used would be to set a current range from zero to a maximum value and the pro-

vided digital code would set the current level within this range. The principle of operation is shown in ***Fig. 3*** where the design uses a common anode RGB LED. The required LED current would be user set by loading a digital code that represents the value of the current within the current range. This would be the code for use in a PWM signal generator circuit that creates a signal with an average value of the required current.

The LED driver circuit design considered in this paper would be considered as a custom design for the sensor application and should be seen in the context of alternative approaches. With the increased use of LED lighting in commercial and domestic applications, a range of commercial devices are available and could be used instead of developing this custom design. However, the requirement in this work was to design and develop a custom mixed-signal electronic circuit using the PLD and discrete analog components for prototyping with the aim to create a design architecture that had the following attributes:

1. The same design could be implemented using a CPLD or FPGA with discrete analog components as well as within a custom ASIC design using a standard +3.3 V CMOS fabrication process.
2. The creation of a design that could be integrated into an ASIC solution to provide for a physically small and hence more portable electronic circuit. In this case, the intention was for the design to operate as part of a portable OFS system.
3. Consideration of the sensor system design with the requirements for its intended application(s).
4. Identification of design requirements for the discrete and ASIC approaches that could be used in other sensor system designs. Here, design reuse was to be an important consideration.
5. Identify existing LED driver circuit designs that could be used as an alternative and their key functions. Commercial designs would be designed for specific purposes and incorporate functions that would not be required in certain designs. Hence, a consideration in this work was to consider the specific requirements for the sensor system.

Therefore, whilst an existing commercial device could have been used in this design study, the intention was to develop a custom design for the sensor system that requires an RGB LED light source.

Table 1 identifies five different commercial devices available and specific key device functions of interest in this work. The TLC5940 and LP55281 devices from Texas Instruments would incorporate functions of most interest in this work.

Table 1: *Example existing commercial products.*

Device	Key device functions
TLC5940 (Texas Instruments) 16-Channel LED Driver With DOT Correction and Grayscale PWM Control	16-Channel LED Programmable current Constant-Current Sink of 0 to 60 mA or 0 to 120 mA 12-bit PWM 3 V to 5.5 V SPI serial communications
LP55281 (Texas Instruments) 12-Channel RGB/White-LED Drive With SPI, I^2C Interface	4, RGB LEDs Programmable current Separate power supply voltages for different parts of the device SPI or I^2C communications
CAT4101 (On Semiconductor) 1 A Constant-Current LED Driver with PWM Dimming	1 LED (or multiple LEDs in series) PWM input signal Up to 1 A set by external resistor 3.0 V to 5.5 V
STCS2A (ST Microelectronics) 2 A max constant current LED driver	1 LED (or multiple LEDs in series) PWM input signal Up to 2 A set by external resistor 4.5 V to 40 V
TL4242 (Texas Instruments) TL4242 500-mA, Adjustable, Constant-Current LED Driver	1 LED (or multiple LEDs in series) PWM input signal Up to 500 mA set by external resistor 4.5 V to 42 V

3.2 System operation

In order to make the design more useful, programmable current ranges would be set using externally connected current sensing resistors with values set according to the LED current requirements. In a typical arrangement, the PWM signal would be at 0 V and +1 V levels and the value of the resistor would set the maximum LED current when a +1 V d.c. level was set. Hence, for a 10 mA maximum current, the resistor would be 100 Ω. Similarly, for a maximum current of 100 mA, a 10 Ω resistor would be used. The current level can be adjusted by controlling the PWM signal's duty cycle. It is possible to either manually switch resistor values or to incorporate a digitally controlled analog switch arrangement whereby a digital code sent from a host processor would open or close particular switches to set the resistor value. However, the electrical characteristics of the switch would then need to be carefully selected for correct circuit operation.

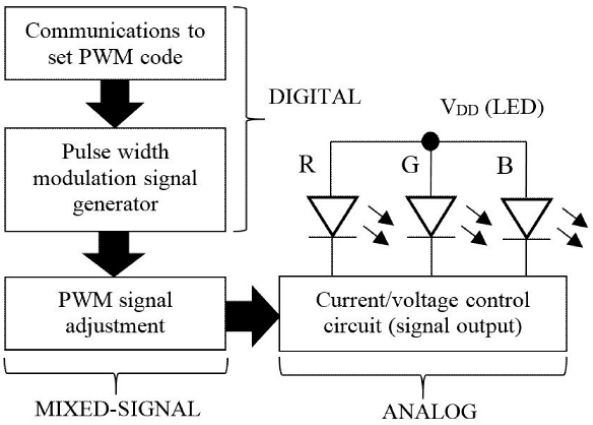

Fig.3: *RGB LED driver overview.*

Within a circuit implementation, the extend of close matching between the required and actual cur-

rent levels would be dependent on the tolerance in value of the current sensing resistor, the voltage levels of the PWM signal, the stability of the PWM signal frequency, values and tolerances of other passive components used in the circuit and the output voltage dynamic range of an operational amplifier (op-amp). To create the current control, the following typical set-up would be used:

1. The current range would be set by the use of the current sensing resistor
2. The user programs the PWM code which sets the current level required within the set current range
3. The user programs whether the PWM code is applied directly to the LED or whether it is firstly low-pass filtered to provide a d.c. current level
4. The user programs any offset value to adjust for variations in passive component values (i.e., the tolerance in value of the resistors used) and variations in the power supply voltage from the nominal value

The circuit then automatically updates the PWM signal, the PWM signal adjustment circuitry provides a small adjustment to the user set PWM signal and each LED would be independently controllable. The PWM signal is generated by a digital counter circuit and the digital logic levels (0 and 1) being voltage levels (GND = 0 V and V_{DD} = +3.3 V, respectively) is output to the LED directly or via signal conditioning circuitry that would modify the voltage levels as well as low-pass filter the PWM signal to produce a d.c. level. The principle is shown in ***Fig. 4***. Here, a PWM signal with 25% duty cycle is low-pass filtered to produce a d.c. level.

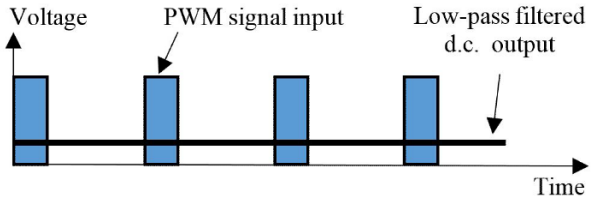

Fig.4: *Principles of PWM - digital input and analog output signals.*

Although d.c. and PWM control of the LED current is of concern in this paper, it is also possible to consider alternative control schemes. For example, both pulse frequency modulation (PFM) and pulse density modulation (PDM) schemes could also be utilised in this arrangement and would require only a change in the initial creation of the encoded signal and the manner in which it was implemented in hardware. ***Fig.5*** shows the principles of the driver circuit for a single LED. Both the digital and analog circuitry would operate on a single +3.3 V power supply for compatibility with low-voltage electronic systems. In the top view (*a*), current control is achieved via an op-amp, bipolar junction transistor (BJT) and current sensing resistor.

The voltage output from the PWM signal conditioning circuit would be applied to the non-inverting input of the op-amp that is acting as a unity voltage gain buffer except that the inverting input is connected to the BJT emitter rather than the op-amp output directly. The BJT acts as a current amplifier and the op-amp negative feedback connectivity will ensure that the voltage across the resistor (R_{SENSE}) follows the op-amp non-inverting input voltage. The transistor allows for the op-amp to drive higher current electrical loads than its own output circuity would allow for. With the power supplies to be used (i.e., +3.3 V for the circuitry except for the LED V_{DD} that, due the high forward voltage of the LED, would be +5 V), the op-amp would need to be a rail-to-rail output op-amp design (capable of an output voltage as close as possible between GND (0 V) and V_{DD} (+3.3 V)). It would also need to have sufficient bandwidth to react to the required PWM signal.

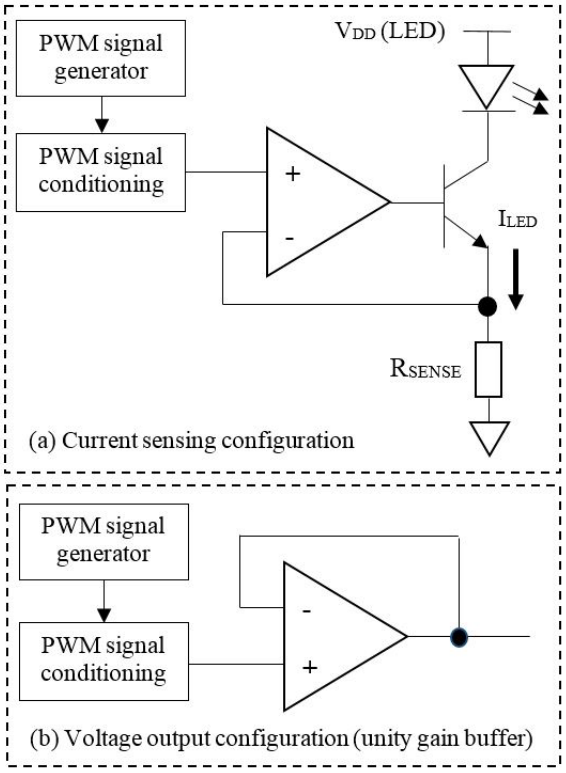

Fig.5: *RGB LED current sensing (top) and voltage output (bottom) circuit configurations.*

The LED current is created by a current source using the BJT as the current source component, requiring the use of the op-amp and current sensing resistor. In an ASIC form, a constant current source typically uses a transistor current source arrangement and this may be physically smaller than the presented

arrangement here. Hence, it should be noted that when considering an ASIC form, it is possible to form the current source differently to the circuit considered here. The PWM frequency would initially be set to a 1 kHz that would provide for a suitable current resolution and avoid the need for high digital clock frequencies. However, applications may need to operate at higher frequencies and so this need should be factored into the design. The BJT could also be replaced with a suitable metal oxide semiconductor field effect transistor (MOSFET) if required. In the bottom view (b), the device outputs a voltage rather than a current and the op-amp is configured to act as a simple unity gain voltage buffer.

The attainable output current levels possible from the op-amp in configuration (b) are therefore limited. Hence, this arrangement would be aimed for use where any circuitry at the op-amp output would require a voltage level with low current requirements. For example, where the output is to control a transistor switch arrangement or where alternative LED current source circuitry were to be used. Both of the above arrangements are possible by suitable design of the overall electronic circuit and the use of analog switches that allow for the signals between the PWM signal conditioning circuit and op-amp non-inverting input to be switched according to the required circuit configuration.

4. ELECTRONIC CIRCUIT DESIGN AND SIMULATION

4.1 Introduction

The RGB LED driver circuit architecture is shown in ***Fig. 6***. This would connect to a host system such as a microcontroller with communications via the serial communications interface, a master clock and an asynchronous active low master reset. The clock frequency utilized was initially set to 1 MHz though with the potential to be increased or decreased. The maximum clock frequency limit is set by the maximum possible operating frequencies of the circuitry. On power-up or a master reset, the design establishes its default operating arrangement. With the design, the digital and analog parts were developed separately and, subsequently, brought together for final integration.

The work considered in this paper relates to the design, simulation, prototyping and characterization of the system with the aim to develop an ASIC version of the mixed-signal design using a suitable low-cost CMOS fabrication process. An IC implementation would reduce the physical size of the circuit, aiding higher levels of integration of the sensor system and portability of the electronics. If the electronic module were to be physically small and use a standardized interface, this would enable the module to be used in a range of different sensor systems. Hence, the design of the electronics was undertaken with the aim to develop both a discrete version and an integrated version using +3.3 V digital CMOS logic.

4.2 Creating the design

In order to create the design, the following tools and techniques have been utilized:

1. Digital circuit design part: The design has been developed using the VHDL hardware description language (HDL) [12]. The design has been created, simulated, synthesized and physically implemented using the Xilinx ISE tools targeting the Xilinx Coolrunner-II XC2C256-TQ144 CPLD [13].
2. Analog circuit design part: Circuit simulation was undertaken to confirm the operation of the circuit and aid selection of the discrete component values using the LTSpice circuit simulator [14].
3. Physical prototyping using discrete circuit components. This involved physical prototyping using solderless prototyping boards (for initial work although with a limited electrical performance) and with a custom printed circuit board (PCB).

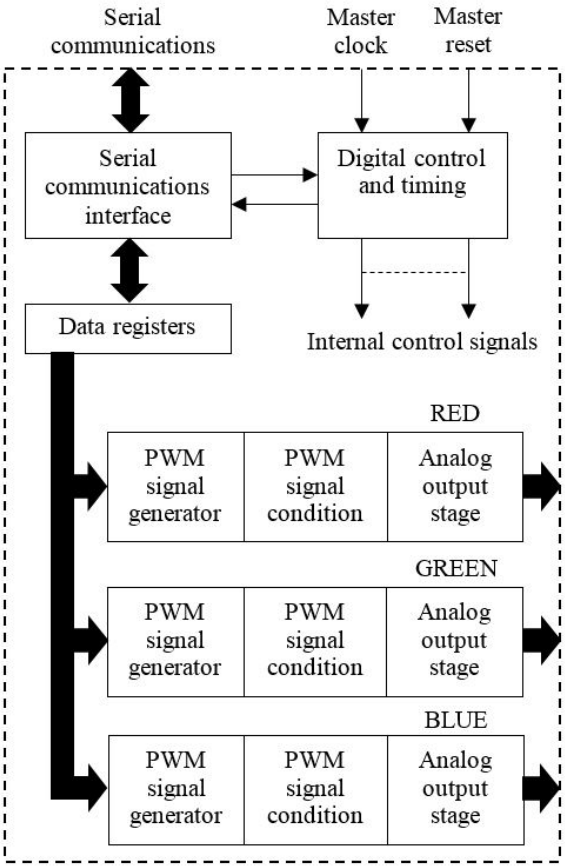

Fig.6: *LED driver circuit architecture.*

4. Design specification for an ASIC implementation using a 0.35 μm mixed-signal CMOS fabri-

cation process [15]. The design entry tools (Cadence Virtuoso), analog simulation (Cadence Spectre) and fabrication process (Austria Mikro System 0.35 μm CMOS) used were accessed through the European Union (EU) Europractice scheme.

Each step was undertaken to verify the operation of the circuit and to gain a better understanding of the circuit requirements prior to committing to an ASIC implementation. In the final ASIC design, the choice as to which of the required circuit components could and should be integrated would need careful consideration to avoid unnecessary cost and to avoid a potential loss in flexibility by limiting the ability for device reconfiguration. The serial communications circuit is based on the serial peripheral interface (SPI) which is a simple synchronous interface suited for short distances and widely used in serial data communications between ICs on a PCB.

Being easy to use and requiring only four pins (i.e., serial clock (SCK), master out slave in (MOSI), master in slave out (MISO) and slave select (SSn)) allows for a simple and efficient serial communications protocol. With the digital logic operating on a +3.3 V power supply, the digital input/output cells used are based on Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) standard. For this, the CPLD input/output cells were configured with this standard (in the Xilinx User Constraints File (UCF), this was set with the command `IOSTANDARD = LVCMOS33`).

4.3 Programmability

The device would have sixteen data registers as identified in ***Table 2*** with each register capable of storing eight bits of data. **Register 0** holds an identification (ID) code for the particular design (a part number in the upper nibble and a part version number in the lower nibble). **Registers 1** to **6** hold the PWM code and offset value for each LED color. **Register 7** will enable or disable the PWM signal offset control.

Registers 8 to **15** provide additional user control and data as follows:

- **Register 8** selects whether each LED color receives a d.c. value (low-pass filtered PWM signal) or the PWM signal directly
- **Register 9** selects whether a low or high voltage level is received by each op-amp. It sets the analog switch positions for the resistor-capacitor network to allow for either the full PWM voltage level (0 V/+3.3 V typical levels) or a reduced PWM voltage level (0 V/+1 V typical levels). For typical use, the +1 V level is used for the calculations of the LED currents. In addition, a passive resistor-capacitor (RC) low-pass filter will create the d.c. voltage output.

Table 2: *System programmability.*

REGISTER ADDRESS	DATA REGISTER FUNCTION
0	Device identification (DevID)
1	Red LED current level code
2	Green LED current level code
3	Blue LED current level code
4	Red LED current level code offset
5	Green LED current level code offset
6	Blue LED current level code offset
7	Offset disable/enable
8	LED d.c. or PWM signal
9	LED Low/High voltage range
10	Blank LEDs (disable op-amp output)
11	Internal clock frequency divider
12	TBA (default to test signal outputs)
13	TBA (default to test signal outputs)
14	TBA (default to test signal outputs)
15	TBA (default to test signal outputs)

- **Register 10** disables the op-amp output (BLANK).
- **Register 11** will provide an internal clock frequency divider (e.g., divide by 2).
- **Registers 12-15** are not yet assigned (TBA - to be assigned). These registers are actually used to output test data via the SPI interface to enable internal signals to be monitored, though can be reassigned if needed.

However, given the range of possible configurations, it is then important to have suitable default values which would reduce the risk of incorrect use, potential confusion by the user and a potential damage to the circuit at power-up or circuit reset. The default values are therefore set to:

1. DevID register selected
2. Output code = 0
3. Offset = 0
4. Offset disabled
5. d.c. output and low voltage range selected
6. BLANK LEDs disabled
7. Clock divider OFF

The PWM signal generator was designed to generate the PWM signal in unit steps from 0 to 100 representing 1% increments from 0% to 100% of the output range. The offset control provides for small adjustments to the programmed PWM signal value before it is applied to the PWM signal conditioning circuitry, as represented in ***Fig. 7***, which is controlled using **registers 8** and **9**.

The PWM signal generator provides the variable duty cycle PWM signal at 0 V / +3.3 V levels with a set frequency of 1 kHz derived from a 1 MHz clock. Essentially, the PWM circuit is a counter that outputs high/low levels based on the received values for the LED current level code and the current level offset code. The resistor values are set to enable the +3.3 V level to be reduced to a +1 V level and also to enable the PWM signal to be low-pass filtered in order to construct the d.c. level. The switches en-

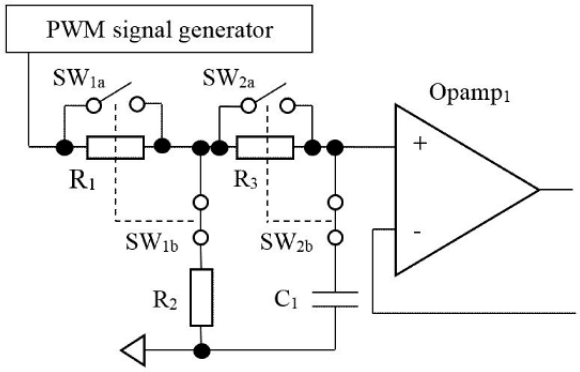

Fig. 7: *PWM signal conditioning circuit.*

able the user to set the output signal type (PWM or d.c.) and whether a +3.3 V or +1 V level is provided. It was decided to use this set-up to give the user flexibility in the use of the circuit for different signal generation requirements. The choice of the resistor values was made based on the analog circuit requirements and also the ability to fabricate the resistors as integrated resistors in the chosen CMOS fabrication process (which supports integrated high-resistance polysilicon resistors).

4.4 Output stage - analog circuit simulation

With a default setting, the PWM signal conditioning circuit and analog output stage would resemble the schematic as shown in ***Fig. 8***. This simulation model was built using LTSpice with discrete component models. The waveform below the schematic shows a PWM input (0 V/+3.3 V typical levels) with a 50% duty cycle (bottom waveform). The middle waveform shows the voltage applied to the op-amp non-inverting input that is a d.c. voltage at 0.5 V due to the 50% PWM duty cycle and low-pass filtering. The capacitor used in the simulation (100 nF) is however a large value and unrealistic if it was a requirement to integrate the capacitance within an ASIC. The size of the capacitor could be reduced by increasing the PWM frequency, changing the resistor values or accepting a higher ripple of the output voltage. The top waveform shows a current of 50 mA through the resistor Rsense (a 10 Ω value giving a range of current from 0 to 100 mA). ***Fig. 8*** shows the PWM signal from the digital circuit being conditioned by the circuit in ***Fig. 7***. The d.c. voltage does include a ripple on the output which needs to be set by the component values based on the ripple voltage that can be tolerated within the design. Hence, the RC network can be made more sophisticated and other component values may be used should alternative output signal characteristics be required. However, the component values and the number of components used must be considered in relation to the physical size of the discrete design and the ability to integrate components within an ASIC solution. The component values chosen here were to integrate the resistors (apart from the current sensing resistor) within the ASIC and to use an external capacitor due to the size of the capacitance required.

In this study, the PWM generation circuit and op-amp are powered by a +3.3 V power supply. Both circuits operate on a single rail power supply, so the op-amp output can vary between 0 V and +3.3 V only.

The RGB LED, showing one LED only in this circuit, is required to operate with a higher power supply due to the voltage drop across the blue and green LEDs. The forward voltage drop for a red LED is around 2 V for a 20 mA forward current. For the green and blue LEDs, the forward voltage drop is around 3 V for a 20 mA forward current.

4.5 Digital logic

The digital logic part of the design was created using VHDL design entry techniques and each VHDL module was instantiated into a top level design schematic as shown in ***Fig. 9***. Each of the VHDL modules and the top level schematic were simulated using VHDL test benches before attempting to synthesise the design and configure the CPLD. Although a particular CPLD was the target device in this application, the VHDL based design could be retargeted to another CPLD or FPGA as the VHDL code itself is device independent as it was written without reference to specific target hardware. In ***Fig. 9***, the design was partitioned into nine functional modules for communications, internal control, configuration setting storage and output. There are three instances of the *PWM_Generator* module that provide the controllable PWM signal for each LED. Whilst this parallelism of hardware (each instance of the *PWM_Generator* module works independently) requires more hardware than a sequentially operating design, it allows for parallel operations and the additional hardware requirements are readily incorporated into the CPLD. This approach is also compatible with targeting an ASIC solution.

In Fig. 9, the individual design modules are:

1. **SPI module** for digital communications.
2. **Clock divider module** to internally reduce the master clock frequency.
3. **Register module** to hold the configuration. This is volatile memory and as such, must be reprogrammed whenever the circuit power supply has been reset.
4. **PWM Generator module** to generate the PWM code according to the values held in the registers. There are three instances of this module, one instance per LED color.
5. **Select Test Output** module to allow for internal values to be viewed via the SPI interface.
6. **Device Identification (*DevID*) module** to

PWM output circuit simulation model in LTSpice where R_1 = 23.25 kΩ, R_2 = 10 kΩ, R_3 = 32 kΩ and C_1 = 100 nF for a 1 kHz PWM input signal with a 50% duty cycle. The digital circuit providing the PWM pulses is modelled as a pulse voltage source.

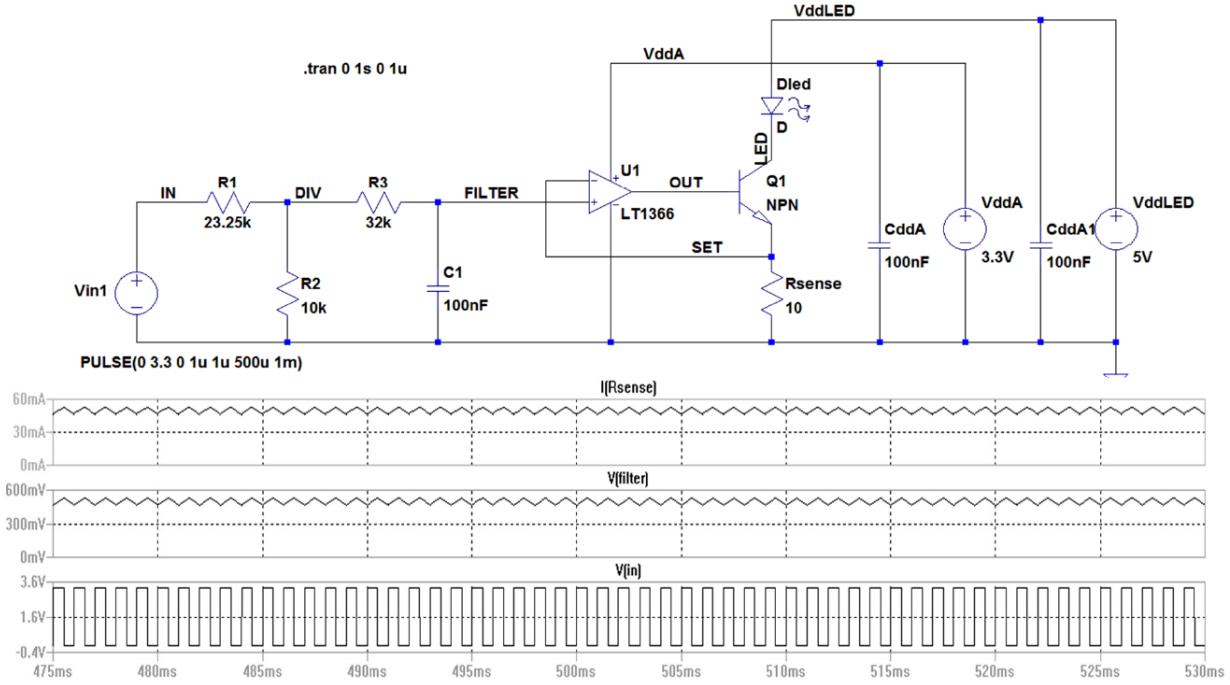

Fig.8: *Output circuit simulation example.*

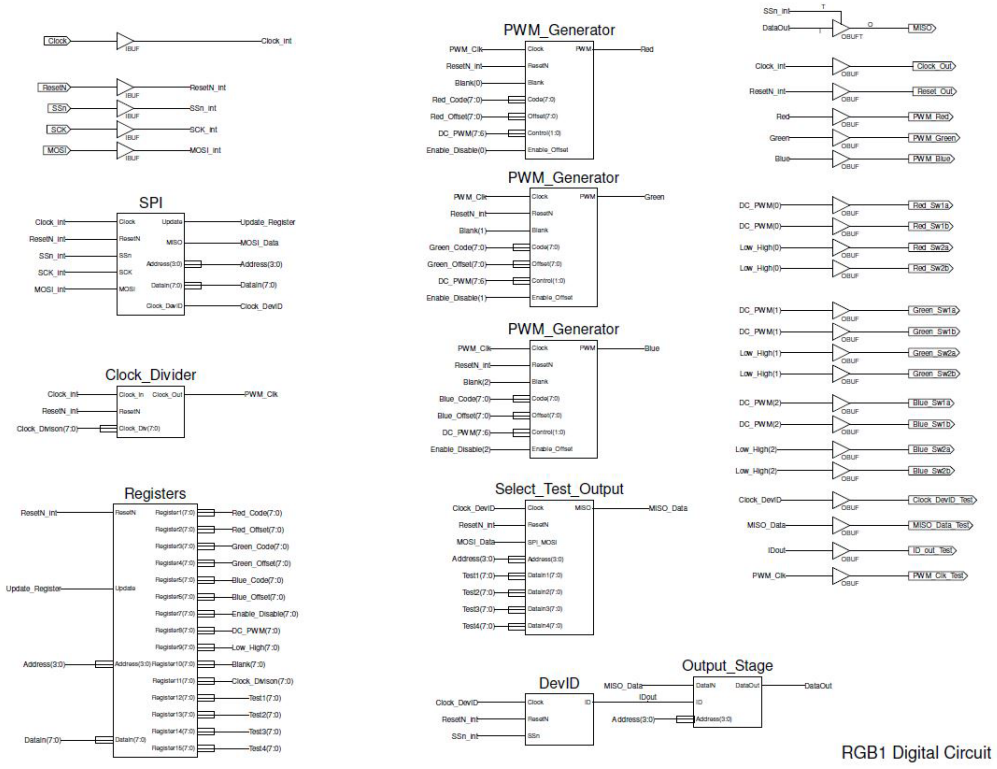

Fig.9: *Digital part - top level schematic in Xilinx ISE.*

hold the identification code of the circuit.

7. **Output Stage module** to set-up the MISO output of the SPI interface.

Each of the VHDL modules and the top level schematic were simulated using VHDL test benches and operation verified before attempting to synthesise the design and configure the CPLD.

Table 3 provides a summary of the results from the design synthesis and fitting to the XC2C256-TQ144 CPLD where the CPLD was operating on a master clock frequency of 8 MHz.

The design is however readily targeted to another CPLD or FPGA by reassigning the device and I/O pin placements. The CPLD used is a small device with limited resources when compared to the size and resources of the FPGA. An FPGA implementation would enable additional hardware operations such as light detector output capture (in a digitized form via an ADC), storage, analysis and communications with the host processor. Xilinx ISE version 14.7 was used with default synthesis settings, pin positions user defined and all I/O pins set to 3.3 V LVCMOS (low-voltage CMOS) standard.

Table 3: *Synthesis and implementation statistics.*

Device	Resource usage
Xilinx Coolrunner-II XC2C256-TQ144 CPLD	Macrocells Used 238/256 (93%)
	Pterms Used 582/896 (65%)
	Registers Used 154/256 (61%)
	Pins Used 27/118 (23%)
	Function Block 416/640 (65%) Inputs Used

Although the design operation could be simulated, it was also necessary to also verify the operation of the design using physical hardware. The photograph in ***Fig. 10*** shows the first prototype hardware (prior to a final PCB level implementation). The CPLD operates on a +3.3 V power supply and is shown to the top right of the image on a Digilent Coolrunner-II Starter Board [16]. This connects, via voltage level shifting circuitry (5 V to 3.3 V level translation), to an Arduino UNO microcontroller board (bottom left) [17]. The Arduino UNO microcontroller board acts as the host processor and also communicates with a connected computer. The analog output circuitry, excluding the analog switches in the version of the prototype shown in ***Fig. 10***, is located on the solderless breadboard to the top left. Information is also displayed on the liquid crystal display (LCD, bottom right) to provide user feedback on the host processor status. The RGB LEDs used were driven with a maximum current of 20 mA. Hence, a 50 Ω sensing resistor (5 × 10 Ω resistors with 1 % tolerance) was required. The op-amps required a high slew rate in order to provide a fast transition from a low to a high voltage when providing the PWM signal current directly in order to ensure that the digital code was accurately represented. This would be particularly important for higher PWM frequencies and when using alternative encoding techniques such as PDM.

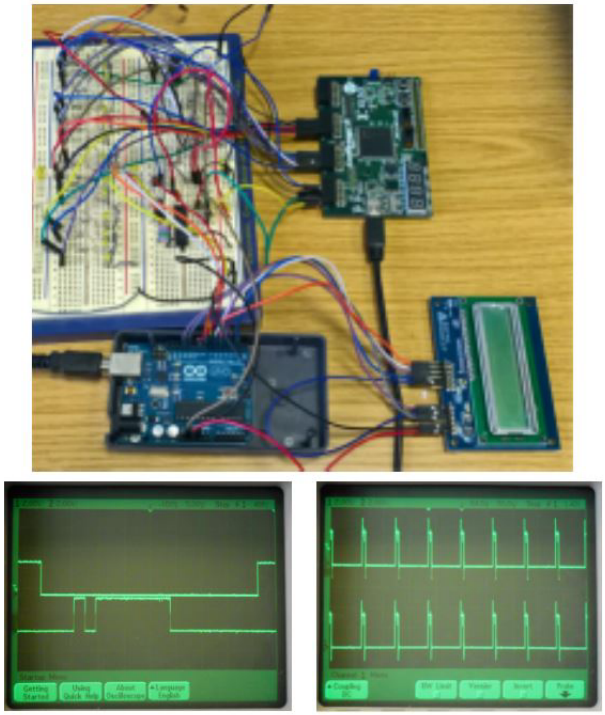

Fig.10: *First prototype hardware with signals viewed: left (example SSn and MOSI signals) and right (example red and green LED PWM signals).*

5. CMOS ASIC CONSIDERATIONS

5.1 Introduction

In this paper, the design architecture and principles of operation of the circuit design have been introduced and discussed. The aim here was to identify the main building blocks for this programmable RGB LED driver circuit with a role to operate as the transmitter within an optical fiber sensor system and to identify design issues relating to discrete and ASIC implementations of the design. The work discussed in this paper has considered the design, simulation and prototyping of the system using discrete components. This would provide for a working solution that could be used directly if designed onto a suitable PCB. However, the ultimate aim of the work was to identify the requirements for and to develop the concept for an ASIC implementation of the design, integrating as much of the circuity as practical such that the physical size of the circuit could be reduced. For example, the circuit uses three op-amps (one op-amp per LED color) which, in discrete op-amp packages, occupy a significant PCB area, even when using surface mount packaging. Hence, integrating devices such as the op-amps, analog switches and resistors would immediately provide for an area

saving. The design of a custom mixed-signal circuit that can be implemented both in discrete component and integrated circuit forms has been considered. The digital circuit was prototyped in programmable hardware that could be either CPLD or FPGA devices. However, as previously identified, with the LED constant current source circuit then it would also be possible to utilise existing, commercial devices. With the increased use of LED lighting in commercial and domestic applications, the range of available LED driver circuits is increasing. For example, the *TLC5940* from Texas Instruments [18] is a *16-Channel LED Driver With DOT Correction and Grayscale PWM Control*. It incorporates a digital serial interface, a programmable maximum LED current of 120 mA using an external resistor and 12-bit PWM current control. The *CAT4101* from ON Semiconductor [19] is a *1 A Constant-Current LED Driver with PWM Dimming*. It can support up to 1 A maximum current and receives a PWM current control input from the user. Therefore, there would be a choice as to what target technology to use and then to use the appropriate technology for the application. The work completed here had an important aim in that it provided additional understanding into the technology options and implications of the choices made.

5.2 Circuit integration

Fig. 11 shows the architecture of the design considered as an ASIC solution. This mixed-signal design would operate on a single +3.3 V power supply for both the digital and analog circuits. The ASIC design described in this paper was developed as a schematic and evaluated using an analog circuit simulator. The layout considerations and evaluation of a fabricated device are not considered. However, as a packaged IC, the design would require a minimum of 19 pins:

- 2 digital power supply (DV_{DD} and DGND).
- 2 control (Clock and ResetN).
- 4 SPI communications (SSn, SCK, MOSI and MISO).
- 2 analog power supply (AV_{DD} and AGND).
- 9 analog pins for the three LEDs (3 pins per LED).

As the high current signals would be "$off-chip$" and controlled by an external transistor, the limited number of power supply pins would be sufficient in this case. However, the use of more power supply pins would be required if higher current levels were considered "$on-chip$". The circuitry inside the dotted area represents the circuitry that would readily be integrated. The digital circuitry would be straightforward to integrate by either synthesising the existing VHDL code or by designing the digital logic directly. Standard digital logic library cells provided with the process design kit have been used as it would not be necessary to design custom digital logic cells. The analog and mixed-signal parts of the design would however need to be designed as full-custom cells. Considering the op-amp circuit itself, this circuit that would be placed on the silicon die within the package would be significantly smaller in surface area than the packaged op-amp device. This could be readily integrated with other analog circuitry and the digital circuitry to form a mixed-signal ASIC. However, there would be a cost associated with designing and fabricating such an integrated design.

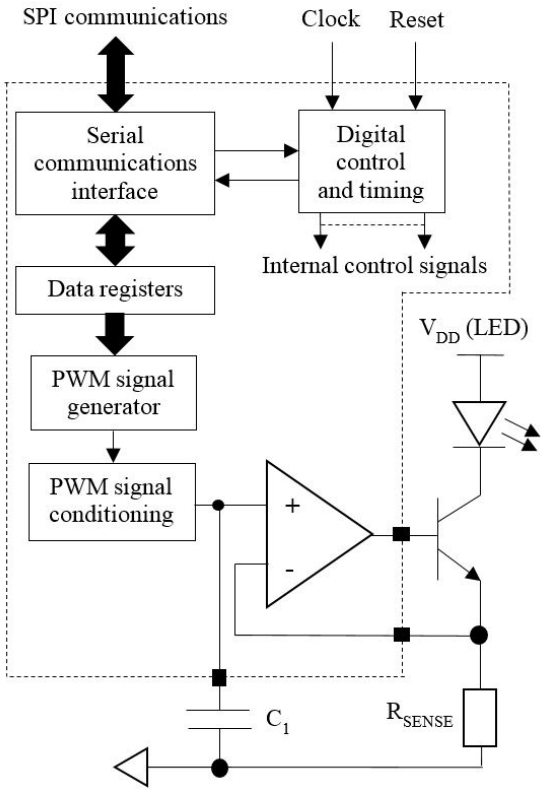

Fig.11: *ASIC design: principle of circuit integration (showing one LED output only).*

With the current control output mode of operation, the transistor is shown here "$off-chip$". If a suitable fabrication process was available, supporting suitable "$on-chip$" power electronic components then the transistors could also be integrated. A process that allows for low- and high-voltage operation, along with the integration of power transistors, would be required. Use of such a process would depend on cost and the ability to reconfigure the circuit operation. However, the current levels involved and the need to switch output signals would need to be considered. The current sensing resistors remain "$off-chip$" to allow for their values to be changed, although if an "$on-chip$" resistor arrangement were possible within the fabrication process then digital control via the SPI of "$on-chip$" resistor values could be used using a resistor and analog switch arrangement. The host processor connections are shown in ***Fig. 12***.

Once the LED driver circuit (the *slave*) has been selected by asserting a low level on SSn, the first set of four clock signals set the register address ($A3-A0$) and the second set of eight clock signals set the register data ($D7-D0$). Both the address and data values are applied using the $MOSI$ signal and are stored in the slave on the rising edge of the clock signal SCK. The third set of eight clock signals outputs internal signals from the slave and are monitored by the master using the $MISO$ signal. These values are valid on the falling edge of SCK. The $MISO$ output is a tristate signal and so can be set to a high impedance state as well as producing logic 0 and 1 levels.

The analog switch used to set the op-amp input signal would be implemented in CMOS using a CMOS transmission gate (TG) as shown in ***Fig. 13***. Each switch uses an nMOS and pMOS transistor with minimal gate length (i.e., 0.35 μm) and a transistor width set according to the required ON resistance value required for the switch so that the maximum switch ON resistance is within an allowed value. The lower the switch ON resistance, the wider the transistor gate widths that are required. The switch connections between A and B are controlled by the logical value on the ON/OFF control input signal. With this type of solid-state switch, the switch ON resistance is dependent on the transistor sizes and the value of the applied voltage. The switch ON resistance versus voltage is of the shape shown in ***Fig. 14***.

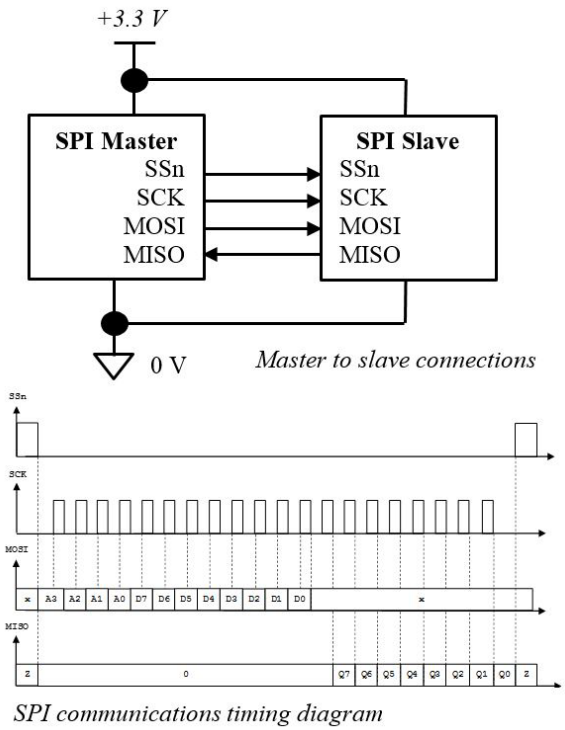

Fig.12: *SPI communications: system programming and internal signal monitoring.*

This resistance is non-zero, varies with switch input voltage (considering node A as the input signal node and the voltage is applied between A and GND) and is a maximum when the switch voltage is between the GND and V_{DD} values.

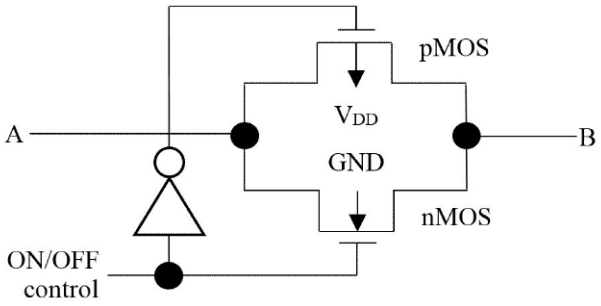

Fig.13: *CMOS analog switch.*

Additionally, switch capacitance and charge injection issues arise if the switch is to be used in a dynamic switching arrangement as would be seen in switched capacitor circuits. However, here charge injection would not be an issue as the switches are set prior to use and so the switching arrangement is considered to be static (i.e., the switch settings are initially applied and any transient signals due to transistor switching are not present).

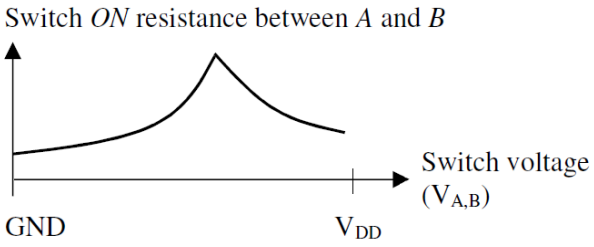

Fig.14: *CMOS analog switch ON resistance versus voltage characteristic.*

The ASIC design was created as a hierarchical schematic design using the Cadence Virtuoso Custom IC Design Environment (version IC 6.1.7). ***Fig. 15*** shows the analog switch schematic that is the schematic representation of ***Fig. 13***.

This switch was then integrated into the signal conditioning circuit of ***Fig. 7***. The Virtuoso schematic for this circuit is shown in ***Fig. 16***.

Finally, the signal conditioning circuit was integrated into an LED driver circuit consisting of the PWM generator circuit, signal conditioning circuit and op-amp as shown in ***Fig. 17***. The PWM generator circuit was implemented using the digital core logic standard cell library. ***Fig. 17*** shows the driver circuit for one LED and hence this design was instantiated three times.

The size of the ASIC (silicon) die and packaging requirements would determine the cost of the ASIC version and if the cost were excessive when compared to

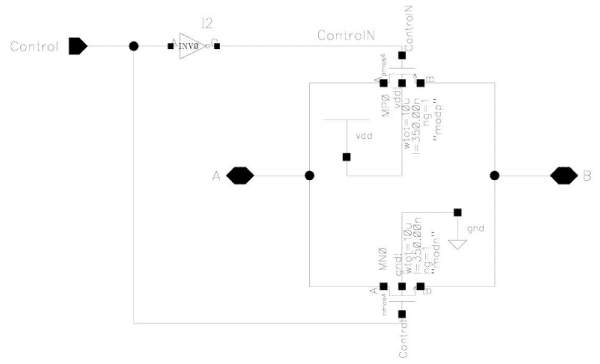

Fig.15: *CMOS analog switch circuit schematic in Cadence Virtuoso.*

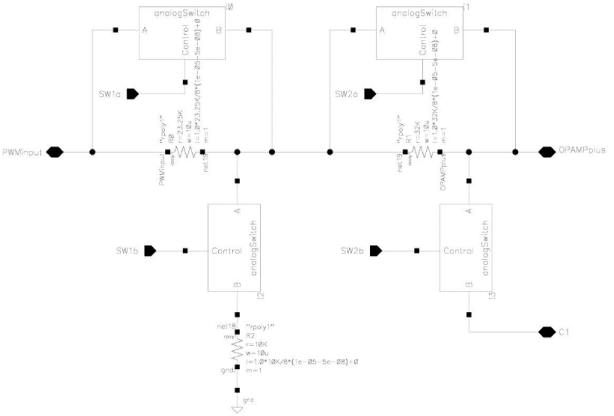

Fig.16: *PWM signal conditioning circuit schematic in Cadence Virtuoso.*

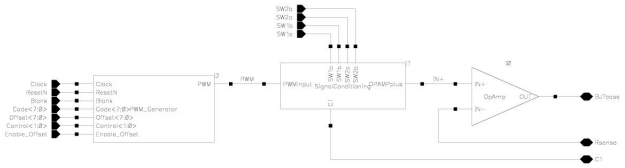

Fig.17: *Analog output circuit schematic in Cadence Virtuoso.*

a discrete version for a particular application, the discrete version would be preferred. The analog switch and integrated resistor arrangement, as depicted in ***Fig. 7***, would occupy a significant area of the silicon die due to number of components required and physical area of silicon that each component would occupy. However, for some applications then the ASIC implementation would be a preferred option irrespective of the cost implications. The overall core circuit design is shown as a schematic in ***Fig. 18***. The partitioning of the design was the same as the CPLD implementation as shown in ***Fig. 9***. However, the key difference between ***Figs. 9*** and ***18*** is that with the ASIC design, the analog signal conditioning circuitry and the op-amps are included in ***Fig. 18***. The final step would be to integrate the core with the periphery pads (signal inputs and outputs) along with the power supply pads

Fig. 19 shows the top level schematic with pad placement in the schematic in the same position as the pad placement. With the requirement for 19 pins, a suitable package would be a 20 pin SOIC (Small Outline Integrated Circuit Package).

The pad placement was arranged to separate the digital and analog parts into separate areas on the die to minimize cross-talk from the digital circuitry into the analog circuitry. The digital pads are placed top and left, and the analog pads are placed right and bottom.

6. CONCLUSIONS

This paper has discussed the design of a mixed-signal and programmable LED driver electronic circuit for current control of a RGB LED to be used in an OFS system. The circuit allows for a number of different design configurations for use in a range of possible optical fiber sensor system transmitter circuits. The architecture for the mixed-signal design was considered for both discrete implementation using discrete components and ASIC solution using a 0.35 μm CMOS fabrication process. The design operation in simulation and the hardware requirements were considered. The paper commenced with a rationale for the RGB LED light source in an optical fiber sensor system as it may provide benefits when compared to a single wavelength light source. The ability to combine wavelengths of red, green and blue light can be used with different sensors to provide additional information on the medium being sensed. The paper then introduced and discussed the design of the circuit chosen for this arrangement and the operation of the analog part of the circuit was presented. The implementation of the digital part within a CPLD and its control of the LED light intensity was then discussed before completing with a discussion into the requirements for an ASIC implementation. The work undertaken here was aimed as creating a flexible LED driver circuit that could be used in a range of OFS systems where the light source was an RGB LED. The design was developed and prototyped as a discrete solution using a CPLD and discrete analog components. The operation of this prototype was evaluated in both simulation and as a physical circuit. Based on verification of the operation of the discrete solution, a CMOS ASIC design was developed and simulated. The evaluation of the ASIC solution in a 0.35 μm CMOS process was undertaken in simulation only.

Future work would consider design layout issues, including evaluation of the design operation incorporating layout induced parasitic components (both resistance and capacitance). Further evaluation would be required before the design could be fabricated and

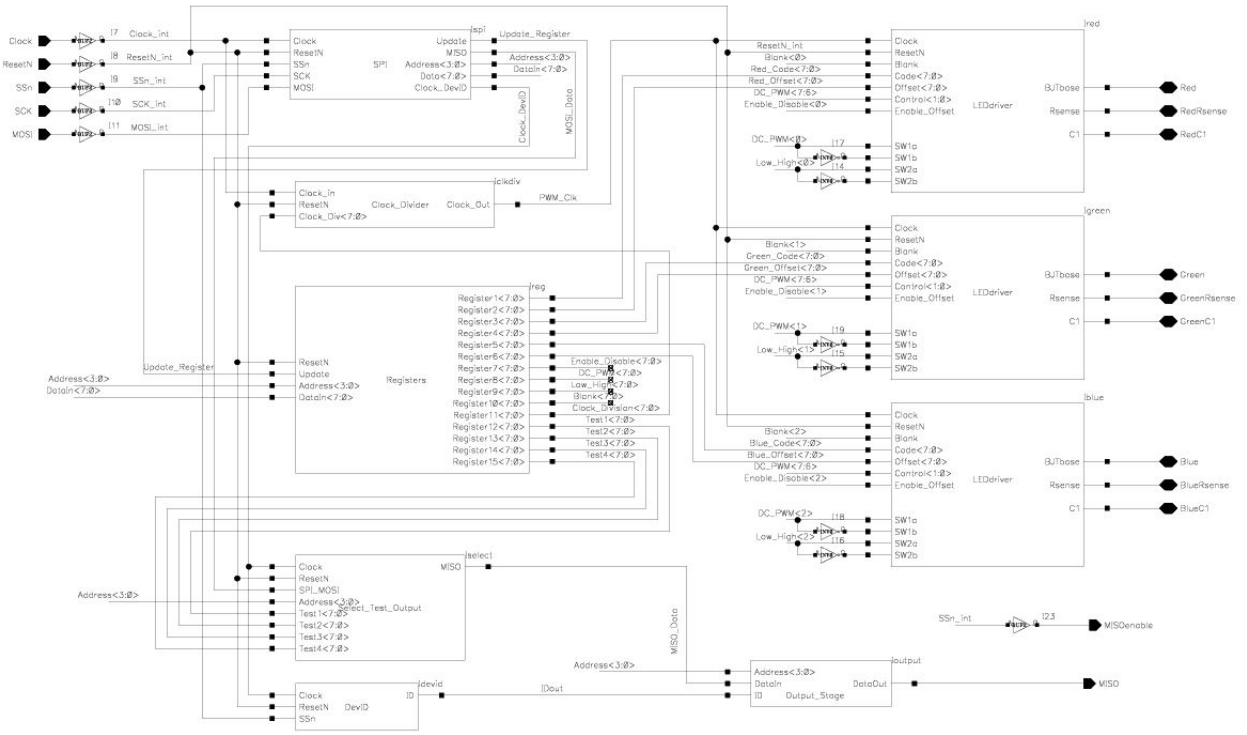

Fig.18: *Core circuit schematic in Cadence Virtuoso.*

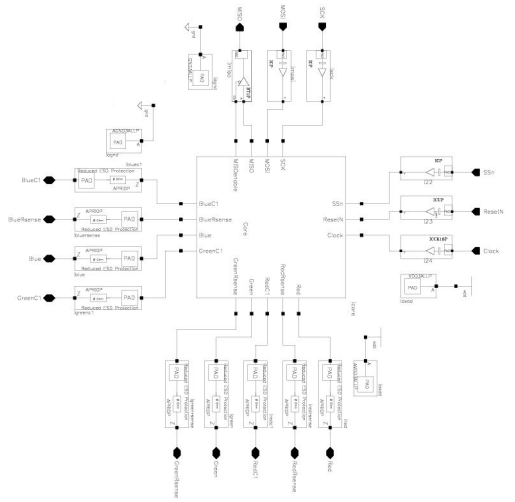

Fig.19: *Top level schematic in Cadence Virtuoso.*

physical testing of fabricated prototypes undertaken.

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