Effects of TiO_2 capping layer on reset current of lateral phase change memory

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ABSTRACT

Lateral Phase Change Memories (LPCMs) gained a lot of interesting due to its simpler fabrication process and lower reset current comparing with vertical-structure phase change memories. The capping layer can be easily fabricated and changed on the active phase-change region of LPCM. The knowledge of capping layer on the thermal generation and diffusion on LPCM can provide an alternative design approach to alleviate the high reset current issue of PCM. The location and thickness of TiO_2 capping layer were studied in order to achieve higher power consumption efficiency using finite element analysis. The four LPCM structures with various location of capping layer were modelled. The simulation results found that addition of TiO2 capping layer can increase power efficiency. The suitable location to place TiO_2 capping layer is at the centre of the active phase-change layer found in Model 4. The thickness of capping layer was developed based on Model 4; and thickness of 40nm was given the best result. The combination of proper location and thickness of TiO2 capping layer can offer a reduction of the LPCM reset current by 24%.

Keywords: Phase Change Memory, LPCM, Reset Current, Finite Element, Structure Design, TiO_2 Capping Layer, Capping Layer Location, Capping Layer Thickness

1. INTRODUCTION

Nowadays, there are the continuously increasing of functionalities and performances of consumer electronic products that are supporting the growing demand for non-volatile memories (NVM) [1,2]. Currently, the most popular NVM is flash memory. Nevertheless, Flash memory is facing severe scalability limitations [3, 4]. New memories have been explored for the next generation NVMs technologies. Phase change memory (PCM) is considered as one of the most promising candidate for next generation NVM technology due to its low power consumption, high scalability, high read/write speeds, long cycle life and good compatibility with standard complementary metal oxide semiconductor (CMOS) processing [5-7]. The PCM cell is stored data by switching the structure of a phase change material, chalcogenide material, typically $Ge_2Sb_2Te_5$ (GST), which can be reversibly switched between the amorphous (high resistivity) and the crystalline (low resistivity) state by Joule heating due to current flow. High reset current is needed to switch the phase change material from the crystalline state to amorphous state (the reset operation). It has become the major barrier for the further scaling of PCM devices. Therefore, reducing the reset current is important issue to reach both high density and low power consumption. Approaches on material design and property can reduce the reset current such as doping with O[8] ,Si[9], N[10] and other elements. The other effective method is to work on the structural design of PCMs. There are several proposed new structure for vertical PCM structure such as edge contact PCM device [11] and μ-trench architecture [12]. Nevertheless, the complication on device fabrication has become the drawback of those complicated structures.

Recently, Lateral phase change memories have gained a lot of interesting due to its simpler fabrication process, easier integration with complementary metal-oxide semiconductor (CMOS) and lower reset current comparing with vertical PCM structure [13-15]. Thus, LPCMs have gained lots of attention particularly on its physical mechanisms. Castro et al. studies the thermoelectric Thomson effect of the different LPCM, such as fine line cell, dog-bone cell and T-cell [17]. Kim et al. presented a mechanism of the electrical switching due to electro-migration effect [18]. Moreover, another approach on additional capping layer, which can be easily fabricated and deposited on the active region of phase change layer have been explored [19-21]. The understanding the effect of capping layer on the thermal generation and diffusion in LPCM is an important issue to design a low reset current LPCM structure; particularly on the type of material, structure, location, and the thickness of capping layer.

In this paper, the location and thickness of TiO2 capping layer were studied in order to achieve higher power consumption efficiency using finite element analysis. The four LPCM structures with various location of capping layer were modelled and studied its

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thermal efficiency. Later on, the thickness TiO_2 capping layer on power consumption efficiency was investigated. Finally, the efficiency of the LPCM with and without TiO_2 capping layer was compared.

2. MODELLING AND SIMULATIONS

LPCM structure with and without TiO_2 capping layer of 90 nm were depicted. Three locations of placed capping layers were investigated at the edge, $^1/_4$ and $^1/_2$ of contact spacing and the LPCM structure without a capping later was used as a reference as Model 1 while the rest were LPCM structure with TiO_2 capping layer of 90 nm at three various locations were labeled as Model 2, 3 and 4. The simulation was carried out using physics-based and Finite Element Simulation (FEM) Program, COMSOL Multiphysics®.

2.1 LPCM Structure

LPCM cell geometry of 90nm node technology was considered and shown in Fig.1 (a). It comprises of 100 nm SiO_2-ZnS film thickness, 30 nm, phase change material ($Ge_2Sb_2Te_5$, GST), and two electrode contacts (titanium nitride, TiN) with thickness of 100 nm. The cell was enclosed by electrical insulating material (silicon dioxide, SiO_2).

Figure 1(b) displayed LPCM with 20 nm TiO_2 capping layer. The location of the TiO_2 layer is defined by d. Three conditions are investigated in the subsequent analysis: Model 2 (d = 0 nm); Model 3(d = 90nm); and Model 4 (d = 180 nm).

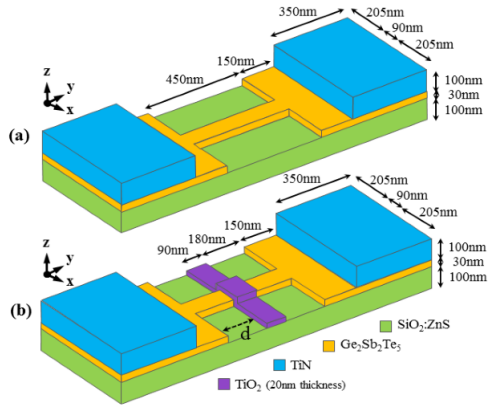

Fig.1: *LPCM model geometry (a) The reference model (Model 1) and (b) The LPCM with capping layer at various locations (Model 2-4).*

2.2 Electro-Thermal Modeling

The temperature profile and current distribution inside the LPCM device were examined. The numerical models were established in the three dimensional (3D) finite element method (FEM) analysis on the basis of the electrical-thermal interaction. During the reset process, a drastic resistance variation of PCMs is attributed to phase-change triggered by Joule heating. The electrical current flows through the LPCM cell, then the heat is generated within LPCM device by Joule heating, which can be expressed as,

$$Q = \rho |J|^2 \tag{1}$$

where Q is the Joule heat induced by current pulse, ρ is the electric resistivity, J is the electric current density and V is the electric potential. The temperature distribution caused by heat transfer in the device can be obtained by solving the heat conduction equation as following:

$$dC\frac{\partial T}{\partial t} - \nabla \cdot (k\nabla T) = Q \tag{2}$$

where d is the density, T is the temperature, C is the volumetric heat capacity, k is the thermal conductivity and t is the time.
The equations (1) and (2) are coupled with Laplace equation:

$$\nabla(\sigma \cdot \nabla V) = 0 \tag{3}$$

where σ is the electric conductivity and V is the electric potential.

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = \frac{1}{D}\frac{\partial T}{\partial t} \tag{4}$$

Where $\boldsymbol{D = \frac{k}{\rho . c_p}}$ is thermal diffusivity and constant k, ρ and c_p are thermal conductivity, density, and specific heat of the materials.

The assumptions for this work are: (a) all of the exterior boundaries were set at room temperature (300K) whereas those of interior boundaries were continuous boundary conditions (b) all of the electrical boundary was set to electrical insulation expect for one boundary of the right electrode set to ground and one boundary of the left electrode where an electrical current pulse was applied to LPCM cell and (c) the material properties used in this study are presented in Table I. These parameters remain constant throughout during calculations.

Table 1: *Physical properties of materials used for the simulations.*

Material	Mass density d(kg/m^2)	Specific heat c_p(J/kgK)	Thermal conductivity k(W/mK)	Electrical resistivity ρ(Ωm)
GST	6200[a]	202[a]	0.46[a]	3.6×10^{-4}[a]
TiN	5240[b]	784[b]	22[b]	1×10^{-6}[b]
TiO_2	4230[e]	711[e]	0.25[c]	1×10^{-2}[d]
SiO_2	2330[a]	730[a]	1.4[a]	1×10^{14}[a]
ZnS-SiO_2	3650[d]	560[d]	0.21[d]	1×10^{17}[d]

[a] Ref. [22] [b] Ref. [23] [c] Ref. [24] [d] Ref. [25] [e] Ref. [26]

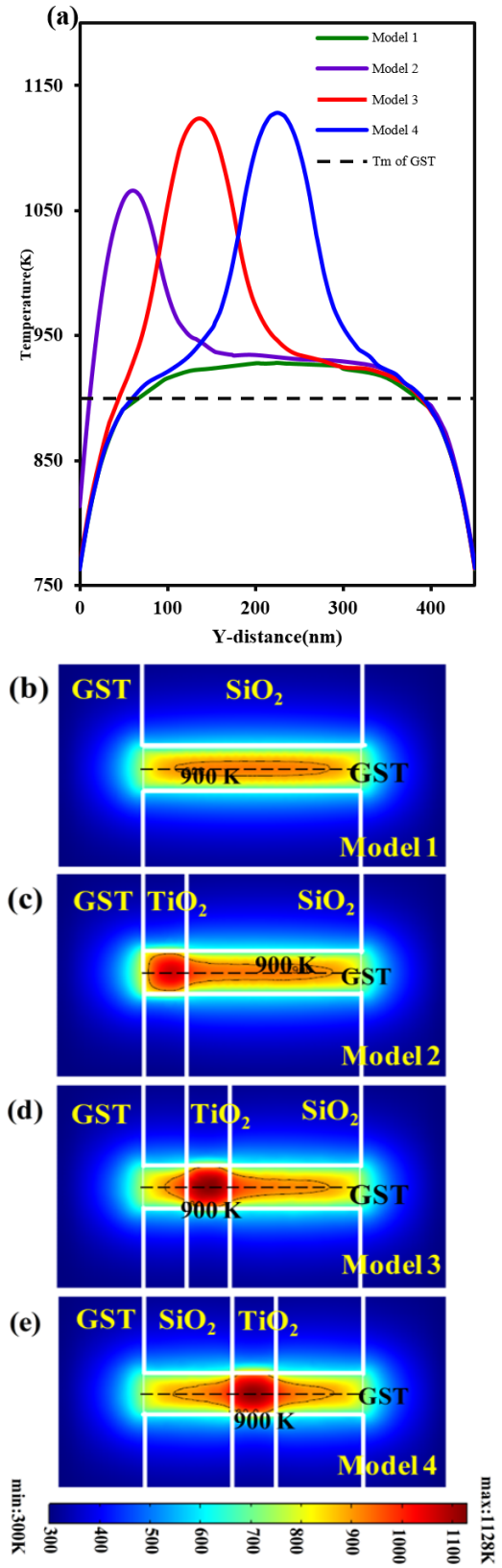

Fig.2: *(a)Peak temperature caused by Joule heating along y-axis (b)-(e) Temperature profile of LPCM cells (Model 1-4) in the cross-section top view(y-axis) with a 104uA and 30 ns current pulse.*

The temperature caused by Joule heating along y-axis of 4 models was monitored and plotted in Fig.2(a) while the temperature profile around the active area were displayed in Fig.2(b)-Fig.2(e).

3. RESULTS AND DISCUSSIONS

The results were classified into two effects of TiO2 chapping layer: Location and Thickness with some discussion on the results.

3.1 Location effect of TiO_2 capping layer on the thermal efficiency

The analysis of LPCM heating efficiency during the reset process through the temperature distribution is very important in order to gain a deep understanding of the LPCM cell operation. The switching of PCM cell to a high-resistance amorphous or reset state requires temperature at the active region beyond melting point (900K). The molten region is an effective programming area which overlaps the entire active region of phase-change layer. This area defined a completion of reset operation.

The location of TiO_2 capping layer targeted to reset current reduction was obtained by performing transient simulation with the same current pulse as shown in Fig 2. Fig.2 shows the temperature profile in each model in the cross-section top view (along y-axis) after applying a current pulse with amplitude of 104 uA and 30 ns pulse width. The comparison of temperature profile shown in Fig.2(b)-Fig.2(e) indicated the proper location to place TiO2 capping layer on the effective programming. Fig.2(a) reveals the maximum temperature of all 4 models. It concludes the proper location of TiO_2 capping layer is at the centre of two contacts (Model 4) which provides the best results comparing with other places.

Moreover, the results in Fig.2 display the effective programming area of LPCM with TiO_2 capping layer is wider than that LPCM without capping layer and smaller when the TiO_2 capping layer is located away from the center active region due to the thermal conductivity of TiO_2 (0.25W/mK) is lower than SiO_2 (1.4W/mK). The additional TiO_2 capping layer on a simple LPCM prevents heat diffusion mechanism at an active phase-change region of LPCM. Then, the active GST cell under TiO_2 capping layer is the peak temperature.

Apart from the temperature caused by Joule heating at the active area should be higher than the melting point temperature of GST material (900K), the completion of active area is able to identify by the boundary of temperature contour of molten as shown in Fig.3. The melting point temperature of GST (900K) was considered as the boundary of cell completion during the reset state. The verification of the cell completion of those four models were carried out by applying the same reset current pattern of 104uA

and 30 ns pulse width to the LPCM with and without capping layer FEM models.

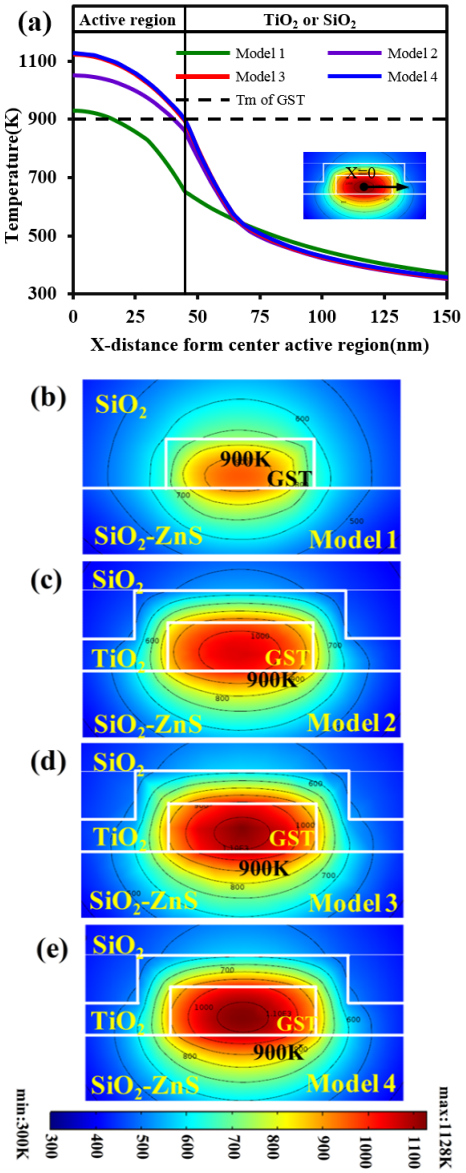

Fig.3: *(a) Peak temperature along x-axis at the effective programming area of each LPCM model with 104uA, 30ns current pulse. (b)-(e) Temperature contour at cross-section view (along x-axis) of Model 1-4.*

The explanation of the proper location of TiO_2 capping layer at the centre between two TiN contacts can be described through the material thermal conductivity. The thermal conductivity of TiN, SiO_2, and TiO_2 are 22W/mK, 1.4W/mK, and 0.25W/mK. The highest thermal conductivity is TiN contact; hence, TiN contacts act as a heat sink as well. The main purpose of adding TiO_2 layer is to prevent heat loss over the active GST area in order to increase the temperature and also widening the active cell or the completion of active cell during the reset state. TiO2 capping layer performs well at the centre area due to its location is the longest distance to TiN contact acting as a heat sink.

Regarding the completion of the active cell during the reset state, the conclusion can be drawn from Fig.3(b)- Fig.3(e). Temperature contour was plotted and the boundary of cell completion was observed using 900K contour line. Model 1 (the reference) and Model 2 show the incompletion of the active GST cell during the reset state with the 104uA and 30 ns current pulse width while the 900K contour line of Model 3 and Model 4 cover the whole GST active area which identify the completion of the reset state. The completion of an active GST area during the reset state reflects the memory cell stability and its retention time.

3.2 Thickness effect of the TiO_2 capping layer on power consumption efficiency

The proper location of TiO_2 capping layer was identified at the centre of the TiN contacts due to the results shown in the previous section. Further reset current reduction was carried out through the study of thickness effect of TiO_2 capping lay on the power consumption efficiency. The optimum thickness was defined as the layer thickness providing the minimum reset current with cell completion during the reset state.

The thickness of TiO_2 layer was varied from 0nm - 80nm with 90nm node technology. The minimum reset current amplitude with cell completion during the reset state was noted at various thickness of TiO_2. The reduction of current amplitude was plotted in percentage using Model 1 as a reference as both results shown in Fig.4.

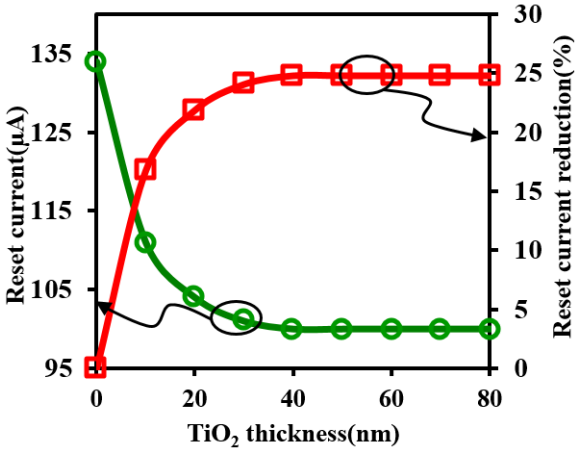

Fig.4: *Reset current as a function of the TiO_2 thickness after applying a 30ns pulse (left). % Reduction of reset current as a function of the TiO_2 thickness after applying a 30ns pulse (right).*

Fig.4 illustrates the reduction in percentage of a reset current as a function of the TiO_2 thickness after

applying a 30 ns pulse (right) while the reset current of LPCM without TiO_2 capping layer was used as a reference. It indicated that the additional TiO_2 capping layer can offer a reduction of the LPCM reset current by 24% with the optimised TiO_2 thickness of 40nm.

The reset current significantly decrease with the increase of TiO_2 thickness in the range of 0-40 nm due to the TiO_2 (0.25W/mK) has lower thermal conductivity than SiO_2 (1.4W/mK). Therefore, the increment of TiO_2 thickness leads to higher thermal resistance of TiO_2, which help to resist the heat transfer to SiO_2 area during the reset state. On the other word, heat loss at the active GST area was reduced; therefore, lower reset current was required to achieve the reset state with completion when the thickness of TiO_2 capping layer increases from none to 40 nm. However, the reset current was saturated with TiO_2 thickness over 40 nm due to the relative large heat leakage into the material is caused by the relative large heat diffusion length of material (Λ) [15,16].

Heat diffusion length of material (Λ) can be described as:

$$\Lambda = \sqrt{D\Delta t} \tag{5}$$

$\Lambda = \sqrt{D\Delta t} \cong 50nm$, where $D = k_{TiO_2}/C_{TiO_2}$ is thermal diffusion constant of TiO_2 material, k_{TiO_2} is thermal conductivity of TiO_2, C_{TiO_2} is the heat capacity of TiO_2 and $\Delta t = 30ns$ is the duration of the constant current pulse.

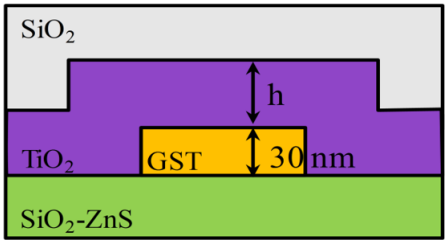

Fig.5: *Geometry in z-axis of LPCM with TiO_2 capping layer.*

Considering the z-axis, GST thickness is 30nm and TiO2 thickness is $\boldsymbol{d}$ = 40nm, the distance from the centre of GST material to the edge of TiO_2 boundary is 55nm (15nm of GST and 40nm of TiO_2) which is the limit of diffusion length of material as calculated in Eq(5). Beyond 40nm, the increment of TiO_2 thickness has played no significance in reset current reduction due to diffusion length of material limitation; hence the optimize TiO2 thickness is 40nm for TiO_2 with the reset current of $\Delta t = 30ns$.

Figure 6(a-b) illustrate the comparison of the temperature profile of LPCM with and without TiO_2 capping layer. It clearly validates the benefit of adding TiO_2 capping layer into a simply LPCM structure

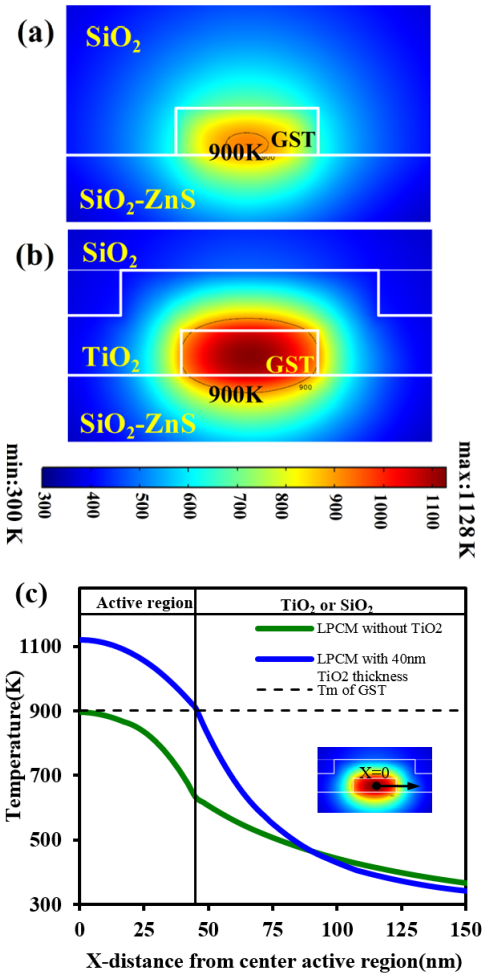

Fig.6: *Temperature profile at the effective programming area of LPCM cells in the cross-section side view (along x-axis) with 100uA, 30ns reset current pulse,(a) LPCM without TiO_2 capping layer,(b) LPCM with a TiO_2 capping layer thickness of 40nm. (c) Temperature along x-axis of LPMC without TiO_2 and with optimised TiO_2 capping layer.*

for the purpose of reset current reduction. Fig.6(c) provides another point of view to display the incompletion of memory cell for the case of LPCM without TiO_2 capping layer.

Fig.7 demonstrates the maximum temperature at the active phase-change region of the LPCM without TiO_2 capping layer and with 40nm TiO_2 capping layer. Temperature rises continuously before becoming saturated during the "on-current" period; and then drop drastically during the "off-current" period. This shows a fast temperature ramping up and down of the LPCM with 40 nm TiO_2 capping layer cell. The the simulation results clearly reveal the maximum temperature of LPCM with 40 nm TiO_2 capping layer cell is approximately 1.2 times higher than the case of the LPCM without a TiO_2 capping layer.

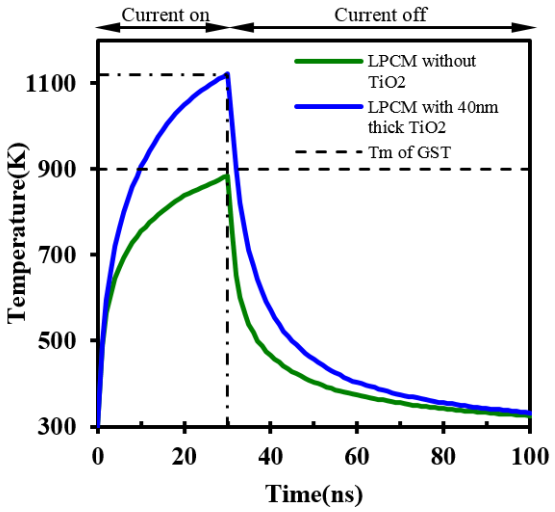

Fig.7: *Maximum temperature profiles for LPCM cell at position in active region with reset current pulse of 100uA and 30ns on current.*

4. CONCLUSION

The simulation results of this work conclude that:

(*a*) Addition of TiO2 capping layer in LPCM can reduce power consumption during data recording

(*b*) The proper location of TiO2 capping layer is at the centre of the active phase-change layer

(*c*) The optimised TiO2 capping layer with 40 nm thickness can offer a reduction of the LPCM reset current by 24%

This signifies a superior performance of the LPCM with 40 nm TiO2 capping layer cell over a simple LPCM without a TiO_2 capping layer.

5. ACKNOWLEDGEMENT

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