RTL Design of Joint CFO and IQ-Imbalance Compensator for Narrow-Band Wireless System

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ABSTRACT

Direct conversion receiver is a well-known receiver architecture that enables small, low power and cheap radio. However, I/Q imbalance caused by non-orthogonality between in-phase component and quadrature-phase component from the imperfections of quadrature demodulator is a major problem in this architecture. In addition, carrier frequency offset (CFO) occurs as well. In this paper, we present a register transfer level (RTL) design of joint CFO and I/Q imbalance compensator. We verify that our system can compensate CFO from -500 Hz to 500 Hz when sampling rate is 9.6 kbps under the effect of I/Q imbalance.

Keywords: Direct Conversion, I/Q Imbalance, CFO, Narrowband Wireless Communication

1. INTRODUCTION

Direct conversion architecture enables small, low power and cheap radio [1]-[4]. Like heterodynes, this receiver uses quadrature mixing but does not have an IF stage. The RF signal is directly mixed to baseband using low pass filters to suppress high frequency interference. Due to zero intermediate frequency, image rejection filters are not needed hence neither bulky surface acoustic wave filters nor high Q analog filters are needed as shown in Fig. 1[5]. However, due to finite tolerances of the analog circuits, the resulting base band signals contain some amount of image interference that limits the spectral efficiency of the system.

I/Q imbalance issues are also very much relevant in direct conversion systems. This I/Q imbalance comes from the imperfection of the local oscillator (LO). When the quadrature waveforms of the receiver is either not perfectly separated by a 90 degree phase or their amplitudes are not exactly the same, it results in I/Q imbalance and it degrades the bit error rate (BER). The carrier frequency offset (CFO) between transmitter and receiver oscillator also degrade the BER.

Recently, various algorithms to estimate CFO and I/Q imbalance have been proposed [6-9]. In [6], the algorithm uses special calibration signals to correct I/Q imbalance but it resulted in a considerably more complex circuit. In [7] and [8], an algorithm for I/Q imbalance compensation in the presence of CFO was proposed. [7] uses the product of received preamble signal for estimating CFO.
However, this method causes CFO estimation error because it doesn't take into account the effect of I/Q imbalance. [8] uses a form of spectral estimation in order to measure the CFO via a line search. The result is then used to estimate I/Q imbalance by applying the linear least squares (LLS) algorithm. Spectral estimation not only incurs high complexity due to numerous matrix multiplications but it is also limited by the resolution used in the line search. In [9], estimation of CFO and I/Q imbalance was done in the time domain. This algorithm performs estimation with low computational complexity. In addition, it reported that the algorithm has higher accuracy than [6] and [8].

In this paper, we propose CFO and I/Q imbalance compensation method for narrow band wireless communication system and implement the algorithm in field programmable gate array (FPGA). The implemented system uses the $\pi/4$ differential quadrature phase shift keying ($\pi/4$ DQPSK) wireless communication system. Specifically, the system is based on ARIB-STD-T61 standard which is a narrow-band digital telecommunication system [10].

To implement our algorithm, we create a simulation model and verify with computer simulation. After that, we implement the system in FPGA. We check that the distorted signal constellation due to CFO and I/Q imbalance is compensated by using our compensation system.

The rest of the paper is organized as follows. Section 2 explains about CFO and I/Q imbalance and mathematical model of received signal on direct conversion receiver. In section 3, we introduce the algorithm used for estimating CFO and I/Q imbalance parameters. The results of computer simulation are discussed in section 4. In section 5, we present our

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proposed circuit and implementation results. Finally, conclusions are given in section 6.

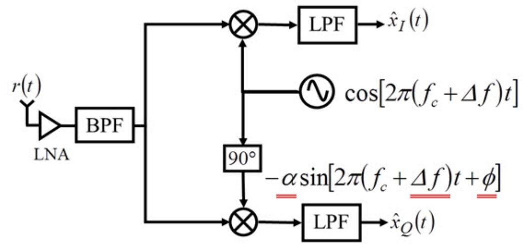

Fig.2: *Architecture of Direct Conversion Receiver.*

2. CFO AND I/Q IMBALANCE

Fig. 2 shows the receiver model when CFO and I/Q imbalance occur. The α and ϕ represent gain imbalance and phase imbalance between an in-phase component and quadrature component respectively.

These are generated by imperfections of the quadrature demodulator. $r(t)$ is pass-band received signal, f_c is carrier frequency, $\hat{x}_I(t)$ and $\hat{x}_Q(t)$ are in-phase component and quadrature?component of received base-band signal, respectively.

A received signal that has been influenced by CFO and I/Q imbalance as shown in Fig. 2 can be expressed by (1) [9][11].

$$\hat{x}(t) = \left\{e^{j2\pi\Delta ft}x(t)\right\}c_1 + \left\{e^{-1j\pi\Delta ft}x^*(t)\right\}c_2 \quad (1)$$

where

$$c_1 = \frac{1}{2}(1-\alpha e^{-j\phi}), c_2 = \frac{1}{2}(1-\alpha e^{j\phi}) \quad (2)$$

3. COMPENSATION ALGORITHM

We use a cyclic preamble signal with a period of N samples and linear least squares (LLS) method for doing I/Q imbalance and CFO estimation. The cyclic preamble signal has $P = (M \times N)$ length is shown in Fig. 3. The CFO and I/Q imbalance compensation model on the other hand is shown in Fig.4. w is a complex parameter for compensating the influence of I/Q imbalance. We positioned w in the I branch of the receiver in order to balance the branches. In [9], w is a filter with L taps because of frequency dependent I/Q imbalance being caused. However, in narrow band wireless communication, I/Q imbalance is only frequency independent. As a result the w should be a scalar parameter in our system. $e^{-j2\pi\Delta ft}$ is a parameter for compensating phase rotation in the received signal by being affected by CFO.

3.1 Estimation of CFO Parameter

In this section, we show the algorithm to estimate CFO parameter. Given M repeated symbols

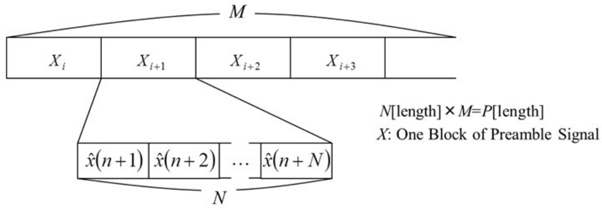

Fig.3: *Cyclic Preamble Signal Model*

are transmitted, samples from (1) can be rewritten as,

$$\begin{gathered}\hat{x}(n+(k-1)N) = e^{j2\pi k\varepsilon}\beta(n) + e^{-j2\pi k\varepsilon}\gamma(n) \\ k = 1, 2, \ldots, M\end{gathered} \quad (3)$$

$$\beta(n) = \left\{e^{j\dfrac{j2\pi n\varepsilon}{N}}x(n)\right\}c_1, \quad (4)$$

$$\gamma(n) = \left\{e^{j\dfrac{j2\pi n\varepsilon}{N}}x^*(n)\right\}c_2, \quad (5)$$

$$\varepsilon = \Delta f T_s N. \quad (6)$$

$(a)^*$ represents the conjugate of a. The parameter ε is the normalized CFO parameter Δf while T_s is the sampling rate. The first three symbols from (3) are

$$\hat{x}(n) = e^{j2\pi\varepsilon}\beta(n) + e^{-j2\pi\varepsilon}\gamma(n), \quad (7)$$

$$\hat{x}(n+N) = e^{j4\pi\varepsilon}\beta(n) + e^{-j4\pi\varepsilon}\gamma(n), \quad (8)$$

$$\hat{x}(n+2N) = e^{j6\pi\varepsilon}\beta(n) + e^{-j6\pi\varepsilon}\gamma(n), \quad (9)$$

Elimination of the first terms of the right hand sides of (7-9), results in

$$\hat{x}(n)e^{j2\pi\varepsilon} - \hat{x}(n+N) = \beta(n)(1-e^{-j4\pi\varepsilon}), \quad (10)$$

$$\hat{x}(n+N)e^{j2\pi\varepsilon} - \hat{x}(n+2N) = \beta(n)(1-e^{-j4\pi\varepsilon}), \quad (11)$$

We proceed to eliminate β and after some algebraic operations, (10-11) will finally lead to

$$2\hat{x}(n+N)\cos(2\pi\varepsilon) = [\hat{x}(n) + \hat{x}(n+2N)]. \quad (12)$$

Due to $\cos(2\pi\varepsilon)$being real valued, the real and imaginary components of the received signal can be independently used to estimate the CFO. However in order to have smaller error variance, both components are used as shown in (14) and (15). Using the LLS, the CFO estimate is thus,

$$\Delta\tilde{f} = \frac{\cos^{-1}\left[(\mathbf{a}^T\mathbf{a})^{-1}\mathbf{a}^T\mathbf{b}\right]}{2\pi T_s N} \quad (13)$$

where

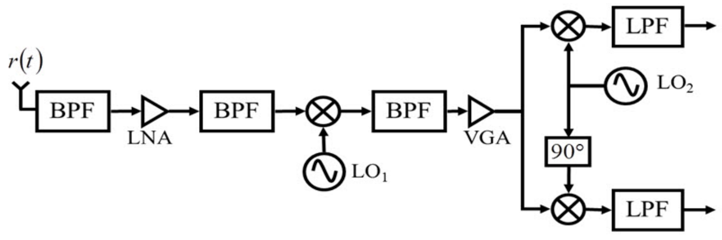

Fig.1: *Architecture of Super Heterodyne Receiver.*

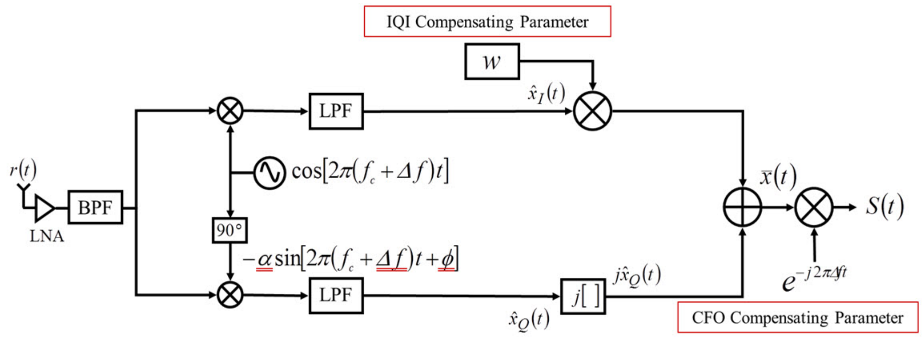

Fig.4: *CFO and I/Q Imbalance Compensation Structure*

$$\mathbf{a} = \begin{bmatrix} 2\hat{x}_I(n+N) \\ 2\hat{x}_Q(n+N) \end{bmatrix} \tag{14}$$

$$\mathbf{b} = \begin{bmatrix} \hat{x}_I(n) + \hat{x}_I(n+2N) \\ \hat{x}_Q(n) + \hat{x}_Q(n)(n+2N) \end{bmatrix} \tag{15}$$

$\hat{x}_I(n)$ and $\hat{x}_Q(n)$ are in-phase component and quadrature component of received base-band signal respectively. We use the coordinate rotation digital computer (CORDIC) circuit function instead of $\tan(\cdot)$ function in implementation phase, so (13) is now rewritten as

$$\Delta\tilde{f} = \frac{\tan^{-1}\left[(\mathbf{a}^T\mathbf{b})^{-1}\sqrt{(\mathbf{a}^T\mathbf{a})^2 - (\mathbf{a}^T\mathbf{b})^2}\right]}{2\pi T_s N} \tag{16}$$

Note that the LLS operation in this instance can be likened to a dot product operation which have very low computational complexity.

3.2 Estimation of I/Q Imbalance Compensation Parameter

In this section, we show the algorithm to estimate I/Q imbalance compensation parameter w [6]. Knowing the value of the CFO (normalized CFO $\tilde{\varepsilon}$), estimation of the compensation parameter w becomes much easier. From Fig. 4, the compensated output $\bar{x}(n)$ is computed as

$$\bar{x}(n) = \hat{x}_I(n) \cdot w + j\hat{x}Q(n) \tag{17}$$

$$\bar{x}(n+N) = \bar{x}(n)e^{j2\pi\varepsilon} \tag{18}$$

It follows from (17) and (18) that

$$\left[\hat{x}_I(n)e^{j2\pi\varepsilon} - \hat{x}_I(n+N)\right] w = j\hat{x}_Q(n+N) - j\hat{x}_Q(n)e^{j2\pi\varepsilon} \tag{19}$$

This is a form solvable by using the LLS algorithm. Thus

$$w = (\mathbf{c}^H\mathbf{c})^{-1}\mathbf{c}^H\mathbf{d}. \tag{20}$$

where

$$\mathbf{c} = \left[\hat{x}_I(n)e^{j2\pi\varepsilon} - \hat{x}_I(n+N)\right] \tag{21}$$

$$\mathbf{d} = \left[j\hat{x}_Q(n+N) - j\hat{x}_Q(n)e^{j2\pi\varepsilon}\right] \tag{22}$$

In equation (20), H represents the Hermitian conjugate.

4. COMPUTER SIMULATION

In this section, we show the results of computer simulation before implementation. Simulation parameter is shown by Table 1. In all of simulations, we use a system based on the ARIB-STD-T61 standard. The modulation scheme is $\pi/4$DQPSK. The training symbol used for all simulations are the 16 short preamble symbols. After these symbols, we insert a random signal which represents actual data. The symbol pattern is [0, 0, 0, 0, ...]. It is mapped on [$\pi/4$, $\pi/4$, $\pi/4$, $\pi/4$, ...] in ARIB-STD-T61 [10]. Simulation was done with the model shown in Fig. 5. Fig. 6 shows accuracy of CFO estimation with mean squared error (MSE) of calculating CFO. We compare the accuracy with method proposed in [7]. Our proposed method is approximately 4 times better than [7] in terms of MSE. Fig. 7 shows bit error rate of

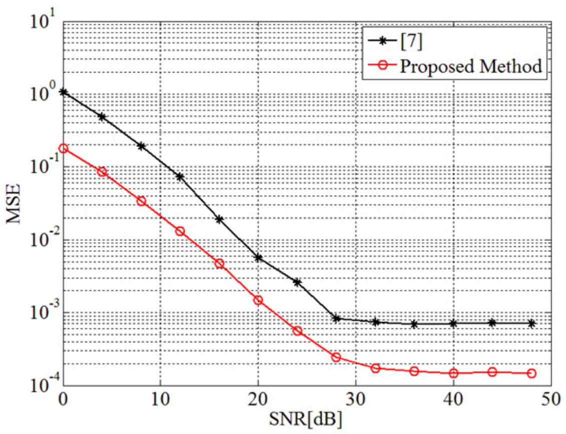

Fig.6: *CFO Estimation Accuracy over Rayleigh Channel ($\alpha = 0.5, \phi = 10deg, \Delta f = 1.25ppm$)*

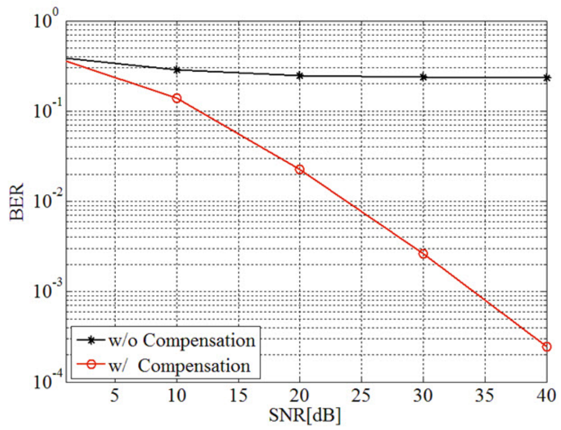

Fig.7: *BER Characteristic over Rayleigh Channel ($\alpha = 0.5, \phi = 10deg, \Delta f = \pm 1.25ppm$)*

our direct conversion simulation system with and without the proposed compensation algorithm. The simulation parameter of Fig. 7 is shown in Table 1. The CFO parameter was varied at 100 Hz intervals inside [-500, 500] Hz. This area is intended as ± 1.25 ppm when 400 MHz defined by ARIB-STD-T61 as carrier frequency is used. We averaged all of BER on each CFO shown above. The performance of compensation system can be seen in Fig. 7. Though the line without compensation has high BER floor due to an influence of CFO and I/Q imbalance, the line with compensation has improved BER. We can say that this compensation system works well from this result.

Table 1: *PSNR and MSE for different filter sizes*

Modulation	$\pi/4$DQPSK
Number of transmitted symbol	5000
Channel	Rayleigh
Iteration	1000
CFO	± 1.25[ppm]
Gain imbalance	0.5
Phase imbalance	10[deg]

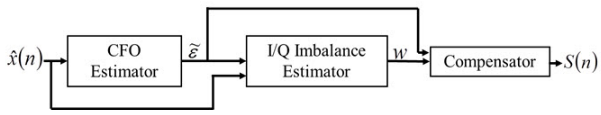

Fig.8: *Compensation Circuit Block Diagram*

5. RTL CONSTRUCTION AND IMPLEMENTATION RESULTS

We have designed a register transfer level (RTL) with model-based design software Simulink [12] and Synphony High-Level Synthesis (HLS) [13]. First, we made a model based design of the compensation system shown by Figs. (8) to (10) on Simulink. Synphony model compiler provides an RTL design from the fixed point model-based design made on Simulink with Synphony HLS.

A compensation block diagram is shown by Fig. 7 and circuits in each block are shown by Figs. (8-10). In Fig. 8, CFO estimator block computes CFO parameter. The I/Q imbalance estimator block needs this estimated CFO parameter for computing I/Q imbalance compensation parameter w.

Received base-band signals $\hat{x}_I(n)$ and $\hat{x}_Q(n)$ are processed as equations (13) to (15) in CFO estimation circuit. An accumulator holds the intermediate results from the calculations using the preamble signals. Fig. 9 shows the I/Q imbalance compensation parameter w estimator circuit. The circuit in Fig. 10 calculates the parameters needed to calculate w. Input signal $\cos(2\pi\varepsilon)$ and $\sin(2\pi\varepsilon)$ can be generated from results of processing in Fig. 9. Thus, this system has to estimate parameter w after CFO parameter and there is some delay to

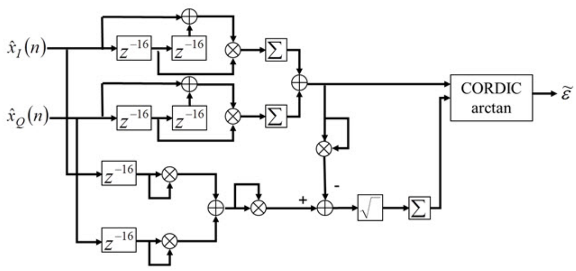

Fig.9: *CFO Estimation Circuit*

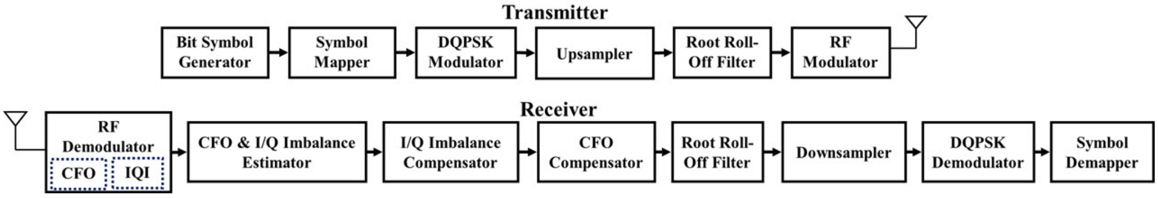

Fig.5: *Simulation System Block Diagram. (This model conforms with ARIBSTD-T61)*

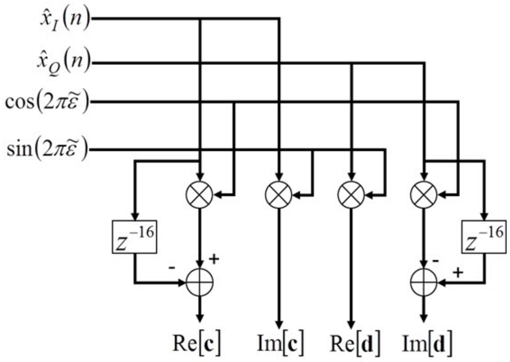

Fig.10: *I/Q Imbalance Estimation Circuit (Front-half)*

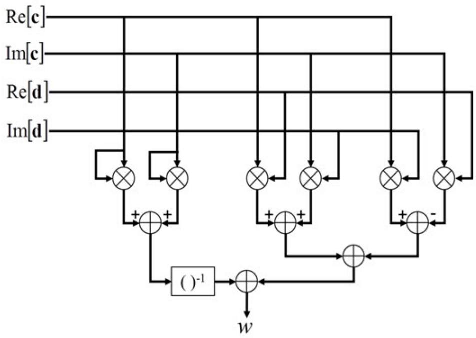

Fig.11: *I/Q Imbalance Estimation Circuit (End-half)*

Table 2: *Target FPGA and Hardware Utilization*

Target FPGA:Xilinx Virtex-5 (XC5VFX70T)		
LUTs	2,828	6%
DSP48E	24	18%
Register	2,385	5%

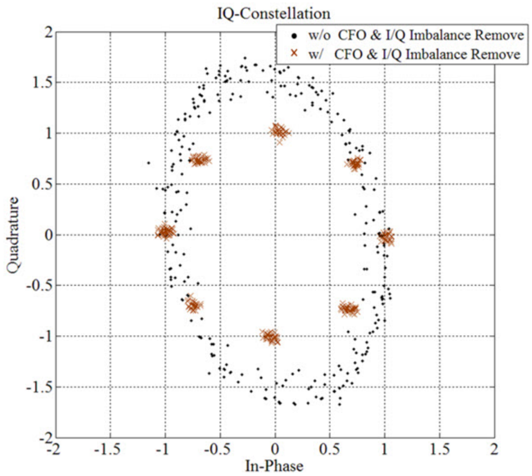

Fig.12: *Constellation on RTL Simulation over AWGN,* $SNR = 20dB, \alpha = 0.5, \phi = 10deg, \Delta f \pm 1.25ppm$

compensate CFO and I/Q imbalance in this system. Output of circuit in Fig.10 is processed by circuit shown by Fig.11, where w is obtained.

We implement the system on FPGA board (Xilinx: Virtex-5 XC5VFX70T) and Table 2 shows implementation results. These utilization data mention only compensation systems with 32 bit width. DSP48E has multiplier and adder circuits and has more than 40 operating modes which are controlled automatically. For example, multipliers, multiply-accumulate unit, power adders, subtractors, three input adder, barrel shifter, wide path multiplexer, wide counters, and comparators can be implemented using DSP48E. The maximum operating frequency of the proposed compensation system is 70 MHz. This operating frequency is enough for ARIB-STD-T61 standard because the standard defines 9.6 kbps as data transmission speed [10].

6. RTL SIMULATION AND FPGA VERIFICATION

The results of the RTL simulation are shown by Fig. 12 and Fig. 13. These simulations are done with Synphony HLS in Matlab 7.9.0. The RTL simulator is constructed according to the model shown in Fig. 5. The influence of CFO and I/Q imbalance was added to the signal based on Fig. 2.

Fig. 12 shows the constellation before and after compensation. In Fig. 12, the symbol $(\cdot)$ show constellation before compensating and thus this constellation has been distorted to ellipsoidal shape due to the I/Q imbalance and been rotated due to the CFO. The symbol $(\times)$ in Fig. 12 shows the constellation after compensation. This constellation is plotted without rotation on well defined locations with proper phase spacing of $\pi/4$ because the influence of CFO and I/Q imbalance has been compensated by the proposed system. Fig. 13 shows the comparison of BER on each bit width. The system constructed with 16 bits-width has error floor when SNR is around 40 dB.

Figs. 14 and 15 show simulation results by using the implemented system. Unlike the model shown in Fig.5, we implemented the system without the "Upsampler",

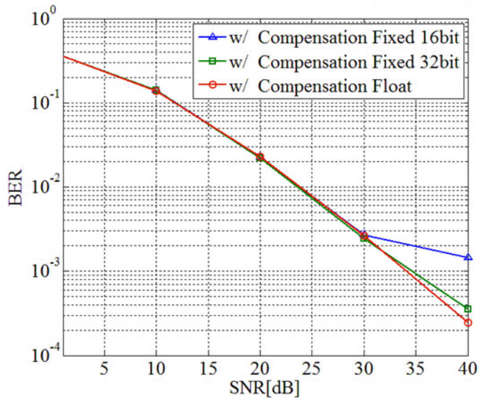

Fig.13: *BER Characteristic over Rayleigh Channel,* $\alpha = 0.5, \phi = 10deg, \Delta f \pm 1.25ppm$

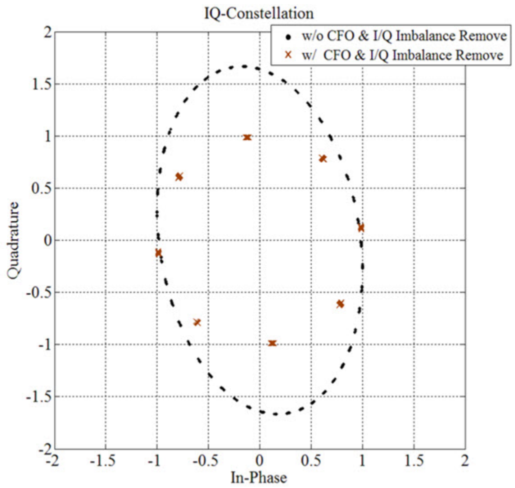

Fig.14: *Constellation on FPGA Verification,* $Nosiefree, \alpha = 0.5, \phi = 10deg, \Delta f \pm 1.25ppm$

"Band Limiter" and "RF modulator" in FPGA and evaluated its system performance. In Fig. 14, the data with compensation has been corrected for the influence of CFO and I/Q imbalance similar to Fig. 12. (a), (b), and (c) in Fig. 15 show binary data before modulation in transmitter, after demodulation in direct conversion receiver, and the result of exclusive-or between (a) and (b), respectively.

7. CONCLUSIONS

In this paper, we have presented an RTL design and implementation of joint CFO and I/Q imbalance compensator for narrow-band wireless system. We have shown that the proposed system can compensate CFO from -500 Hz to 500 Hz when sampling rate is 9.6 kbps and there is the effect of I/Q imbalance. In the future, we will compute BER using a system implemented on FPGA

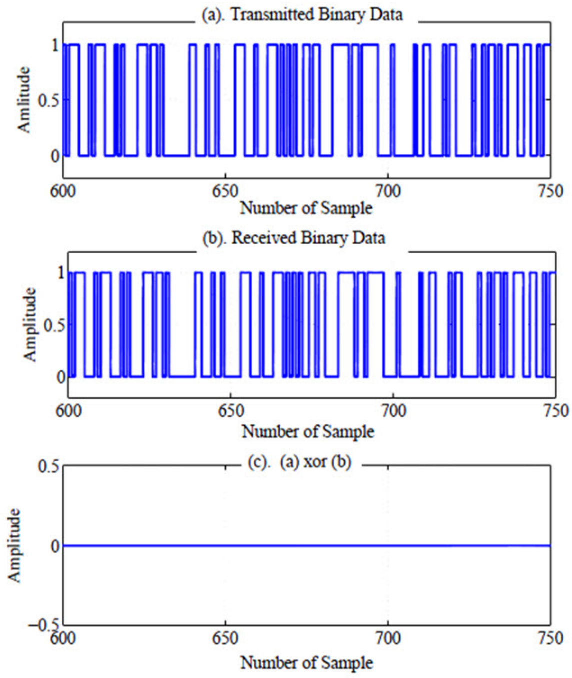

Fig.15: *Input and Output Binary Data,* $Nosiefree, \alpha = 0.5, \phi = 10deg, \Delta f \pm 1.25ppm$

and combine the system on FPGA and RF modulator. Finally, we will examine its perform in an actual field test.

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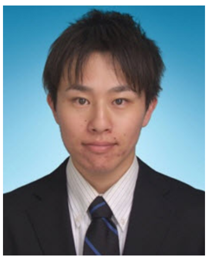

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