Low Power Despreader using Dynamic Reconfigurable Architecture for Multicarrier CDMA with Two-Dimensional Spreading and Variable Spreading Factor

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ABSTRACT

In this paper, we propose a dynamic reconfigurable architecture of a despreader for Multicarrier code division multiple access (CDMA) with two-dimensional spreading and variable spreading factor. The spreading factors in the time and frequency domains are varied according to cell configuration, channel load, and propagation channel conditions in the system. The structure of the proposed despreader is dynamically changed with spreading factors. Following this structure, optimum parallel and pipeline processing are achieved. The proposed despreader reduces the power consumption by 60% compared with the basic one.

Keywords: low power circuit, dynamic reconfiguration, despreader, Multicarrier CDMA

1. INTRODUCTION

Recently, there are various researches of the next generation mobile communications (4G) to establish broadband packet transmission with a maximum data rate exceeding 100Mbit/s [1]-[4]. In 4G system, the seamless deployment of wireless access employing one air interface is required in both multi-cell and isolated-cell environments. Multicarrier CDMA, which is examined to be used in 4G system, is based on a combination of orthogonal frequency division multiplexing (OFDM) signaling and CDMA technique.

The Multicarrier CDMA schemes are mainly categorized into three groups. The first group spreads the original data in the frequency domain [5],[6]. The second group spreads the original data in the time domain [7]. The third group spreads the original data in both the frequency and time domains [8]. In addition, the Multicarrier CDMA with variable spreading factor, which changes the spreading factor corresponding to the cell structure, channel load, radio link conditions and radio link parameters, has been proposed [9]. Although several communication methods of the Multicarrier CDMA with two-dimensional spreading and variable spreading factor have been examined [10]-[12], its hardware design has hardly been discussed. However, it is important to design a small size and a low power consumption circuit when the Multicarrier CDMA is mounted on the mobile terminal such as the cellular phone.

In the Multicarrier CDMA with two-dimensional spreading and variable spreading factor, the module structure that is quit different from a conventional system is a despreader since both spreading factors in the frequency and time domains are changed adaptively. Although the matched filter is usually used for despreading in the direct sequence CDMA [13], we consider that the sliding correlator can process it in the Multicarrier CDMA. In this paper, the sliding correlator is modified for the two-dimensional spreading. Furthermore, the despreader is designed with low power consumption using parallel and pipeline architecture. We have already proposed a dynamic reconfigurable despreader that changes the structure according to the spreading factor [14]. The proposed despreader in [14] can achieve parallelization and pipelining. This paper explains a circuit structure of the proposed despreader, and evaluates the area and the power consumption of the designed circuit.

2. MULTICARRIER CDMA WITH TWO-DIMENSIONAL SPREADING AND VARIABLE SPREADING FACTOR

In the Multicarrier CDMA with two-dimensional spreading and variable spreading factor, the spreading factors in the time and frequency domains, i.e. SF_t and SF_f, are varied according the cell structure in order to achieve higher link capacity in both multi-cell and isolated-cell environments. The configuration of the two-dimensional spreading is shown in Fig.1. One data symbol is spreaded into SF_t successive OFDM-symbols and SF_f successive sub-carriers. A total spreading factor SF is $SF_f \times SF_t$.

Fig.2 shows the baseband processing of the receiver for despreading. The symbol timing is detected and

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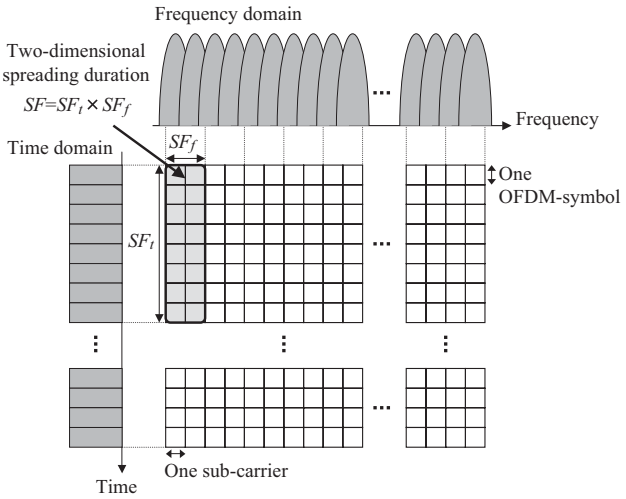

Fig.1: *Multicarrier CDMA with two-dimensional spreading and variable spreading factor.*

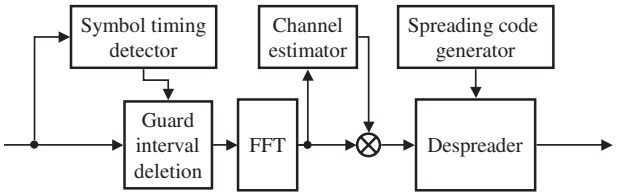

Fig.2: *Baseband processing at receiver.*

the received signals are separated into sub-carrier sequences using Fast Fourier Transform (FFT). After the channel variation of each sub-carrier is compensated, the despreader calculates the correlation between equalization data and spreading code from the spreading code generator.

3. STATEMENT OF PROBLEM

A network system which adapts to both wireless LAN and cellular system can sufficiently be constructed by implementing a variable spreading factor (Fig.3). For example, the Multicarrier CDMA performs the same processing as OFDM used in conventional wireless LAN when $SF = 1$. On the other hand, since the cellular system is under multicell environment, each cell is identified by multiplexed code where SF is set to be greater than 1. Furthermore, the transmission quality can be improved by changing SF_t and SF_f according to the propagation condition [11]. When delay spread σ is large, frequency selectivity fading becomes remarkable. In addition, different amplitudes and phases are influenced on each sub-carrier. Accordingly the orthogonality among the code-multiplexed channels in the frequency domain is destroyed. In this case, smaller SF_f should be employed. When Doppler frequency f_d is large, time fluctuation of fading becomes remarkable. In addition, different amplitudes and phases are influenced on each OFDM symbol. Accordingly the orthogonality in the time domain is easily destroyed. In this case, smaller SF_t should be employed.

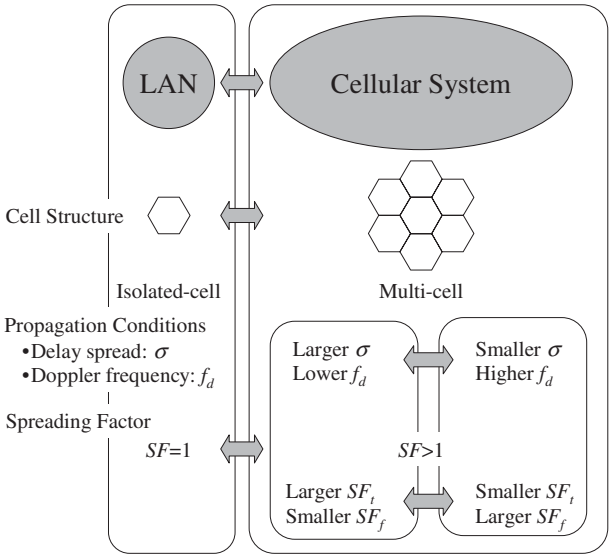

Fig.3: *Concept of wireless network with variable spreading factor.*

Let us consider the situation of mobile wireless LAN. When a user uses his/her system in a room, it may be enough to use conventional OFDM. In this case, SF in the Multicarrier CDMA becomes 1. Once a user moves to cellular environment of Fig.3 with this system, SF should be controlled. Even if the system is used at the fixed location in outside, SF_t should be set large. When a user uses the system in automobile for example, SF_f should be set large.

For hardware design, the mount of (1) microprocessor or digital signal processor (DSP), (2) field programmable gate array (FPGA) or (3) application specific integrated circuit (ASIC), is considered. In the use of microprocessor and DSP, the processing can be changed by software, but the processing performance is insufficient to achieve high transmission rate. In the use of FPGA, the composition of the logical circuit can be freely programmed. The circuit structure is changed suitably according to the spreading factor. However, the transmission rate may decrease when the spreading factor is rapidly changed. This is based on a long time for changing the circuit structure. Therefore ASIC is designed in this paper. The proposed ASIC has high processing performance and instantaneously adjusts to the change of the spreading factor.

4. DESPREADER FOR TWO-DIMENSIONAL SPREADING AND VARIABLE SPREADING FACTOR

As shown in Fig.2, the output of FFT is input to the despreader after the channel equalization. Since the Multicarrier CDMA has many sub-carriers and the real time processing is required, it is suitable to use a pipeline FFT processor. The pipeline FFT processor produces a serial output. It outputs one datum at every one cycle [15]. Fig.4 shows the data flow of an input in a despreader where $d_i(m)$ denotes equalization data of the $i(=0,1,\ldots,N_c-1)$-th sub-carrier at the $m(=0,1,2,\ldots)$-th OFDM-symbol. N_c denotes the number of sub-carriers. If $d_i(m)$ is fed into the despreader at a cycle, $d_{i+1}(m)$ is input into the despreader at the next cycle. This process continues in frequency domain until $d_{N_c-1}(m)$ is finally fed into. The $m+1$-th OFDM-symbol starting with $d_0(m+1)$ is input into the despreader at the next.

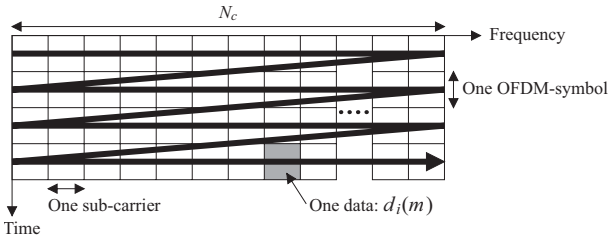

Fig.4: *Data flow of input into despreader.*

After spreading, the data to be transmitted $s_i(m)$ is given by

$$\begin{aligned} s_i(m) &= x(k)c_j(n), \qquad (1)\\ k &= \left[\frac{i}{SF_f}\right] + \left[\frac{m}{SF_t}\right]\frac{N_c}{SF_f}\\ j &= \mathrm{mod}(i, SF_f)\\ n &= \mathrm{mod}(m, SF_t) \end{aligned}$$

where $x(k)$ denotes the data to be transmitted before spreading, and $c_j(n)$ denotes the spreading code. $[X]$ rounds the elements of X to the nearest integers where $[X] \le X$. $\mathrm{mod}\,(Y,Z)$ is the modulus after Y/Z. In the despreader, the following equation is applied.

$$\begin{aligned} y(k) &= \sum_{n=0}^{SF_t-1}\sum_{j=0}^{SF_f-1} d_{f+j}(t+n)c_j(n). \qquad (2)\\ f &= \mathrm{mod}(k, N_c/SF_f)\\ t &= [kSF_f/N_c] \end{aligned}$$

As written above, the despreader processes the non-successive input data in the Multicarrier CDMA with two-dimensional spreading. Accordingly this paper, the simple sliding correlator is used for two-dimensional spreading as shown in Fig.5. It is considered as a basic despreader.

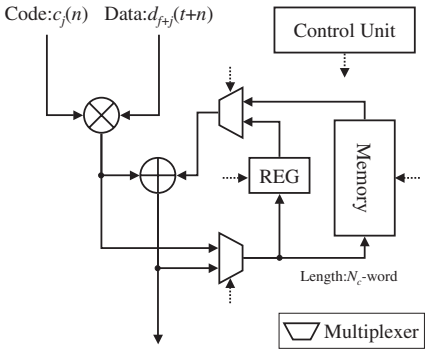

Fig.5: *Structure of basic despreader.*

The frequency domain despreading is processed by connecting the adder and the register as loopback structure in Fig.5. The memory is used to hold intermediate result for the time domain despreading. The maximum capacity of the memory is N_c-words. The actually used area is N_c/SF_f-words.

5. LOW POWER CONSUMPTION DESPREADER

Both parallelization and pipelining of circuit are an effective way of constructing low power architecture [16]. However it is difficult to make a parallel and pipeline despreader of unique circuit structure since the spreding factor SF is changed adaptively in the Multicarrier CDMA that utilizes variable spreading factor. The proposed despreader achieves ideal parallelization and pipelining according to the spreading factor by using multiplexers. Moreover in the proposed despreader, the memory is divided into some small size banks.

An adder network shown in Fig.6 changes connection pattern between add units (AUs) according to the spreading factor in the frequency domain, i.e. SF_f. In the top part of the figure, SF_{max} registers are arranged where SF_{max} denotes the maximum SF_f. The datum is sequentially fed into the adder network. Using these registers, all data are arranged into parallel. These registers work as a serial/parallel (S/P) converter. The adder network consists of SF_{max} AUs, and each AU outputs to the memory. The capacity of the memory of the proposed despreader is N_c/SF_{max}-words. This memory is dual-port. One port is used to hold the output from AU and then to output the calculation result of the adder network. The other port is connected to AU for a loopback structure.

The AU consists of four registers, one exclusive-OR gate and one adder-subtracter as shown in Fig.7. The AU receives as input two spreading codes (Code1, Code2) and two equalization data (Data1, Data2). The outputs of the AU are pseudo code and calculation result (Data Out). Each register holds input data at every SF_{max} cycles. The spreading code used in the Multicarrier CDMA is Walsh-Hadmard

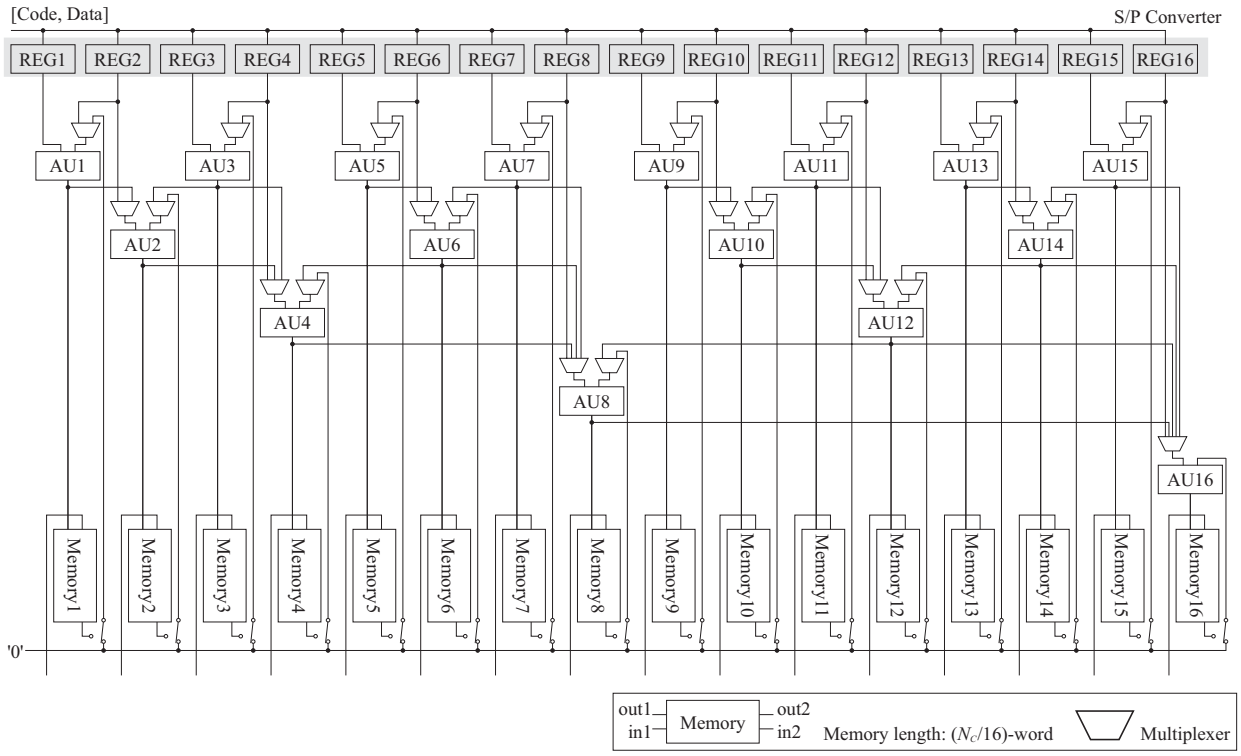

Fig.6: *Structure of adder network ($SF_{max} = 16$).*

code whose value is '+1' or '-1'. Therefore, multiplication between spreading code and equalization datum mentioned in Eq.(2) can be realized to change sign of equalization datum if spreading code is '-1'. The adder-subtracter calculates Data2±Data1. Addition or subtraction is selected according to the output of the exclusive-OR gate. If both Code1 and Code2 are '+1', then addition is selected. The pseudo code thus becomes '+1'. If Code1 and Code2 are '-1' and '+1', respectively, then subtraction is selected. The pseudo code thus becomes '+1'. If Code1 and Code2 are '+1' and '-1', respectively, then subtraction is selected. The pseudo code thus becomes '-1'. The AU accordingly calculates -(Data2-Data1)=Data1-Data2. If both Code1 and Code2 are '-1', then addition is selected. The pseudo code thus becomes '-1'.

Input data of AU are controlled by multiplexer according to several SF_f. In the case of $SF_f = 1$, each AU is composed in parallel (Fig.8(a)). $c_j(n)$ and $d_{f+j}(t+n)$ are input into Code1 and Data1 shown in Fig.7, respectively. In the case of $SF_f = 2$, each AU is composed in two pipeline stages and $SF_{max}/2$ parallel lines (Fig.8(b)). AU of the first pipeline stage processes the despreading in the frequency domain. AU of the second pipeline stage processes the time domain despreading. In the case of $SF_f = 4$, each AU is composed in three pipeline stages and $SF_{max}/4$ parallel lines (Fig.8(c)).

To summarize, the adder network is designed to form the alignment of SF_f AUs in $\log_2 SF_f + 1$ pipeline stages in SF_{max}/SF_f parallel lines. AUs which are arranged from the first to $\log_2 SF_f$-th pipeline stages process the despreading in the frequency domain. The time domain despreading is processed by AU of the last pipeline stage and memory.

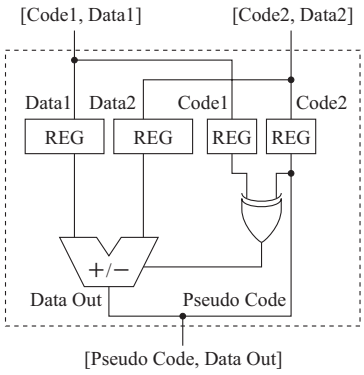

Fig.7: *Structure of add unit.*

Fig.9 shows block diagram of the proposed low power despreader. The control unit generates signals controlling each module. Despreading data is selected from outputs of all memories of the adder network by the parallel/serial (P/S) converter according to the control signal.

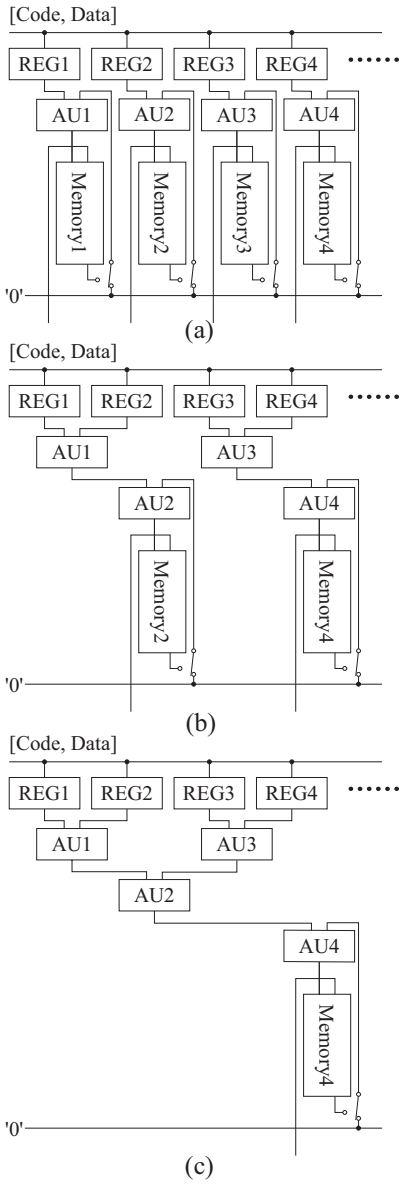

Fig.8: *Connection pattern of adder units (a)$SF_f = 1$(b)$SF_f = 2$(c)$SF_f = 4$.*

6. EVALUATION OF DESIGNED CIRCUIT

Both the circuits of the basic despreader and the proposed low power despreader have been designed with Verilog-HDL and synthesized to TSMC 0.25μm standard cell library with Synopsys Design Compiler. Table 1 shows the design parameters. Since the number of sub-carriers is 768 and the OFDM-symbol duration is 9.259μsec, the cycle of data input to despreader is 12.1nsec. Accordingly, these despreaders are followed by gate level simulations, run at 82MHz. Synopsys Power Compiler is used for power analysis.

Table 2 shows the number of gates. Since the memory is divided into sixteen in the proposed despreader, the number of peripheral circuits of the memory increases more than the basic despreader. Therefore,

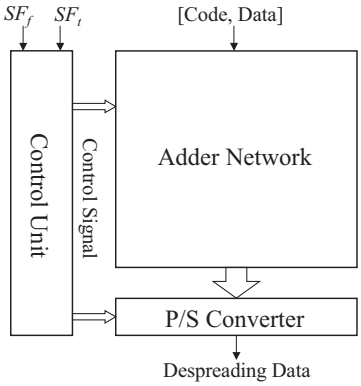

Fig.9: *Block diagram of low power despreader.*

Table 1: *Design parameters.*

Number of sub-carriers, N_c	768
Number of FFT points	1024
Spreading factor, SF	2, 4, 8, 16
OFDM-symbol duration	9.259μsec
Frame length	52 OFDM-symbols (Data:48, Pilot:4)
Input data bits	12bit
Spreading code bit	1bit
Supply Voltage	2.5V

Table 2: *Number of Gates.*

Basic despreader (Memory)	24646 (23478)
Proposed despreader (Memory)	93718 (82630)

the number of total memory gates increases by about 3.5 times. The parallelization and the pipelining also increase the number of the other circuits. The total gates of the proposed circuit increases by nearly 4 times.

Table 3 shows the power consumption. Since in the case of $SF_t = 1$, the memory is not used in the basic despreader, the other circuits, i.e. the multiplier, the adder, the register, multiplexers and the control unit, require the power of 63mw. The clock frequency of proposed despreader is 1/16 compared with the basic one. It reduces the power consumption by 60% or more in the case of $SF_f = 16$ and $SF_t = 1$. In the case of $SF_t \geq 2$, the number of accesses to the memory of the basic despreader increases as SF_t becomes large or SF_f becomes small. As a result, the power consumption increases. On the other hand, the power consumption is constant at any SF_t in the proposed despreader if SF_f is the same. In the case of $SF_f = 1$ and $SF_t = 2$, the reduction of power consumption is the least. The proposed despreader requires 13% less power consumption than the basic one.

Table 4 shows comparison of the proposed despreader with the conventional digital matched filter

Table 3: *Power consumption[mW@82MHz].*

(a) Basic despreader@

	$SF_f = 1$	$SF_f = 2$	$SF_f = 4$	$SF_f = 8$	$SF_f = 16$
$SF_t = 1$		63.2	63.0	62.8	62.7
$SF_t = 2$	93.1	77.6	69.8	66.0	
$SF_t = 4$	110.3	85.2	73.3		
$SF_t = 8$	119.3	89.2			
$SF_t = 16$	123.9				

(b) Proposed despreader

	$SF_f = 1$	$SF_f = 2$	$SF_f = 4$	$SF_f = 8$	$SF_f = 16$
$SF_t = 1$		50.6	35.6	28.2	24.4
$SF_t = 2$	80.7	50.8	35.7	28.2	
$SF_t = 4$	80.3	50.5	35.6		
$SF_t = 8$	80.1	50.4			
$SF_t = 16$	80.0				

Table 4: *Comparison of proposed despreader with conventional DMF.*

	technology [μm]	supply voltage [V]	code length (SF_{max}) [chip]	input data bits	frequency [MHz]	power [mW]	normalized power [μW/MHz/chip]
Proposed	0.25	2.5	16	12		Table 3	
S/P Converter					82	3.0	2.3
AUs					5.2	9.0	108
Conventional[13]	0.18	1.6	256	6		9.3	
Reception Registers					15.6	0.4	0.1
CCB					15.6	8.7	2.2

(DMF) presented in [13]. The proposed despreader has different function from the conventional DMF, i.e., the conventional DMF cannot process the time domain despreading. Moreover, the design parameters, such as the CMOS technology, the supply voltage and the operating frequency, are different. Therefore the proposed despreader cannot easily be compared with the conventional DMF. For rough comparison, the power consumption normalized by the code length and the operating frequency is attached to the same function modules of each circuit. The reception registers and the correlation calculating block (CCB) of the conventional DMF correspond to the S/P converter and the AUs of the proposed despreader, respectively. The power consumption of both the S/P converter and the AUs are constant, regardless of SF.

As the S/P converter is designed by the same architecture with the reception registers, the CMOS technology, the supply voltage and the input data bits become the cause of the S/P converter requiring 23 times as much normalized power consumption as the reception registers. Therefore normalized power consumption of the S/P converter becomes 0.1μW/MHz/chip if it is designed by the same parameter as the reception registers.

The AUs output summation of input data every 193.6nsec in the case of $SF_f = 16$, so its operating frequency is 5.2MHz. The normalized power consumption increases by approximately 49 times compared to the CCB. The ratio of the normalized power consumption of the AUs to that of the CCB is larger than the ratio of the normalized power consumption of the S/P converter to that of the reception registers. The reason for such increase in ratio is that each AU contains registers to keep parallelization and pipelining regardless of SF.

7. CONCLUSIONS

This paper presents a low power despreader for the Multicarrier CDMA with two-dimensional spreading and variable spreading factor. In this Multicarrier CDMA system, the spreading factors in the time and frequency domains are changed according to communication circumstances. Since the structure of the proposed despreader is dynamically changed according to the spreading factor, it can achieve parallelization and pipelining in all the cases. Compared with the basic despreader, it realizes 13-60% power reduction.

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