



Hybrid Approaches for Efficient Simulations of 3-Qubit Quantum Fourier Transform (QFT) Circuit using Quick Quantum Circuit Simulation (QQCS)

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ABSTRACT

The research devised efficient methods for simulating 3-qubit Quantum Fourier Transform (QFT) circuits using Quick Quantum Circuit Simulation (QQCS). The hybrid methodologies suggested as a solution for efficiently simulating the circuit involve the combination of decision diagrams and property exploitation techniques. This paper incorporated two methods based on decision diagrams: the reordering trick and decision diagram approximations, template-based optimization, and linear reversible circuit synthesis for property exploitation. The proposed approaches significantly improved and optimized quantum algorithms and hardware by aiming to simulate quantum circuits accurately and quickly. Simulations using QQCS proved the effectiveness of these strategies, which were then compared to the original circuit. The results yielded valuable insights into enhancing simulation efficiency while upholding circuit accuracy.

Article information:

Keywords: QFT, Hybrid Approaches, Decision Diagram, Property Exploitation

Article history:

Received: July 22, 2023

Revised: October 19, 2023

Accepted: December 28, 2023

Published: April 13, 2024

(Online)

DOI: 10.37936/ecti-cit.2024182.253574

1. INTRODUCTION

In quantum computing, the Quantum Fourier Transform (QFT) is an essential operation that significantly contributes to numerous algorithms like Shor's algorithm for integer factorization [5]. However, the simulation of quantum circuits, including the QFT, becomes computationally challenging as the state space grows exponentially with increasing qubits.

The optimization of quantum algorithms and hardware relies on efficient simulations of quantum circuits. Hybrid strategies combining diverse simulation techniques have displayed the potential to address the computational complexity associated with large-scale quantum circuits [4].

Hybrid methodologies are proposed in this paper to enable efficient simulations of 3-qubit QFT circuits using QQCS. The research introduces the integration of decision diagrams, including the reorder trick, decision diagram approximations, and property exploitation techniques. Designing these techniques aims to

minimize computational overhead while ensuring the precise simulation of quantum circuits. The findings of this research will significantly contribute to the progress of quantum circuit simulation techniques, thereby supporting the advancement and optimization of quantum algorithms and hardware.

Section II organizes the remaining sections of this paper, summarizing related work on decision diagrams and property exploitation in quantum circuit simulation. Section III discusses and uses the specific circuit, detailing the hybrid approaches the researchers will test. Section IV discusses the results obtained from the proposed hybrid approaches. Finally, the paper concludes in Section V.

2. RELATED WORK

This section provides background information on quantum circuit simulation, decision diagrams, and property exploitation in simulations to keep this work self-contained.

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2.1 Quantum Circuit Simulation

Quantum circuit simulation enables the examination and comprehension of quantum system dynamics using computational techniques. It uses a vector representation $[\alpha, \beta]^T$ for single-qubit states, with α and β denoting the probability amplitudes of the states $|0\rangle$ and $|1\rangle$. Simulating systems with N qubits requires taking the tensor product of individual qubit states. While matrix-based operations are employed, traditional array-based approaches suffer from exponential memory consumption. Researchers employ data compression techniques to address this issue, and Decision Diagram-based simulators are considered a promising solution. The simulators depict qubits as nodes and assign probability coefficients to edges in their representation. This method minimizes redundancy by merging states with the same probability amplitudes, improving memory efficiency and computational performance during quantum circuit simulation [1].

2.2 Quantum Circuit Simulation with Decision Diagram

According to Wille *et al.* [1], decision diagrams provide a concise representation and analysis of quantum circuit simulations, enabling efficient depiction, manipulation, and analysis of a circuit's quantum state. Decision diagrams offer advantages in implementing quantum gates, qubit measurement, and calculating measurement outcome probabilities. The authors also propose the utilization of decision diagrams as data structures to tackle the exponential memory

demands in various scenarios.

Shen *et al.* [7] introduced the reorder trick in their paper. This trick reduces the simulation time of a circuit with a SWAP gate at the end. This trick is done by rearranging the gates of the qubits and using a decision diagram. Through this technique, the researchers could explore and study the behavior of quantum circuits even without access to quantum computers.

In related work, Hillmich *et al.* [2] introduced decision-diagram-based quantum circuit modeling, accelerating quantum circuit simulation on classical hardware. This representation method facilitates refined computations and reduces memory demands. However, despite employing decision-diagram (DD) based modeling, the computational intensity of simulating quantum circuits still needs to be improved.

Decision diagrams optimize the simulation of quantum circuits. It not only facilitates the investigation of quantum algorithms and structures but also enables efficient modeling of noise and addressing system faults. Furthermore, it presents various advantages, such as improved expandability, effectiveness, and the ability to simulate noisy circuits more accurately.

2.3 Quantum Circuit Simulation with Property Exploitation

Decision diagrams are not the only available optimization one can use. Researchers also utilize templates to optimize quantum circuits. A template iden-

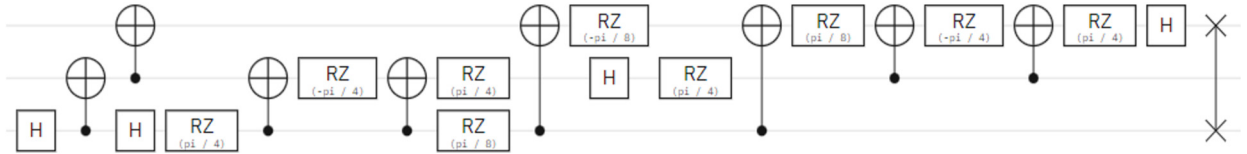


Fig.1: Original Circuit.

```
[ 1] |000>: __H__:C10:C10__: __H__: __Rz(.25):_C10:_Rz(-.25):_C10:_Rz(.25):_H__: __Rz(.125):C20:_Rz(-.125):_C20:_Rz(.125):_Rz(.25):_C10:_Rz(-.25):_C10:_Rz(.25):_H__:Sw02:M3
M1={000:0.25, 010:0.125, 011:0.125, 100:0.213, 101:0.037, 110:0.037, 111:0.213}
[1 0 0 0 0 0 0] __H__C10C10__H__Rz(0.25)_C10_Rz(-0.25)_C10_Rz(0.25)__H__Rz(0.125)C20_Rz(-0.125)C20_Rz(0.125)Rz(0.25)_C10_Rz(-0.25)_C10_Rz(0.25)H__Sw02 [0.278-0.416i 0 -0.069-0.347i 0.347-0.069i 0.09-0.453i 0.188+0.037i -0.106-0.159i 0.384-0.257i]
```

Fig.2: Original Circuit Simulation in QQCS.

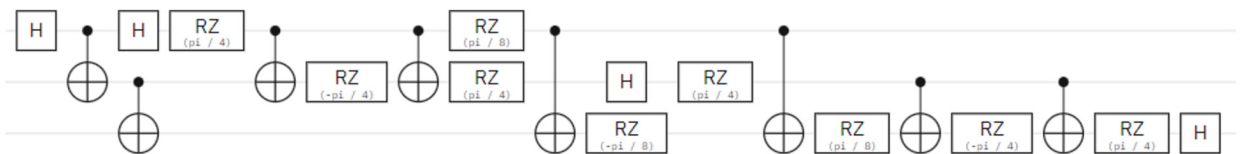


Fig.3: Reorder Trick - Dd Approximation Circuit.

```
[ 2] |000>:H__:C01_:C01:H__: Rz(.25)__:C01_: Rz(-.25):C01_:Rz(.25):_H_: Rz(.125)
5)__:C02__: Rz(-.125):C02__: Rz(.125):_ Rz(.25):_C01__: Rz(-.25):C01__: Rz(.25):_
_H:M3
M1={000:0.25, 010:0.125, 011:0.125, 100:0.213, 101:0.037, 110:0.037, 111:0.213}
[1 0 0 0 0 0 0] H__ C01_ C01 H__ Rz(0.25)__ C01_ Rz(-0.25)_ C01_ Rz(0.25)_ H
_ Rz(0.125)__ C02_ Rz(-0.125) C02_ Rz(0.125) Rz(0.25)_ C01_ Rz(-0.25)_ C01_ Rz
z(0.25) __H [0.278-0.416i 0 -0.069-0.347i 0.347-0.069i 0.09-0.453i 0.188+0.037i -0.
106-0.159i 0.384-0.257i]
```

Fig.4: Reorder Trick – DD Approximation Circuit in QQCS.

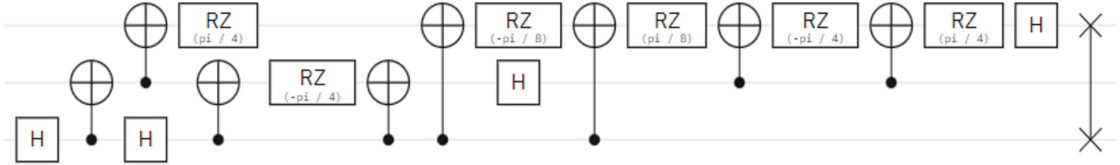


Fig.5: Template-Based Circuit Optimization – DD Approximation Circuit.

```
[ 2] |000>:H__:C01_:C01:H__: Rz(.25)__:C01_: Rz(-.25):C01_:Rz(.25):_H_: Rz(.125)
5)__:C02__: Rz(-.125):C02__: Rz(.125):_ Rz(.25):_C01__: Rz(-.25):C01__: Rz(.25):_
_H:M3
M1={000:0.25, 010:0.125, 011:0.125, 100:0.213, 101:0.037, 110:0.037, 111:0.213}
[1 0 0 0 0 0 0] H__ C01_ C01 H__ Rz(0.25)__ C01_ Rz(-0.25)_ C01_ Rz(0.25)_ H
_ Rz(0.125)__ C02_ Rz(-0.125) C02_ Rz(0.125) Rz(0.25)_ C01_ Rz(-0.25)_ C01_ Rz
z(0.25) __H [0.278-0.416i 0 -0.069-0.347i 0.347-0.069i 0.09-0.453i 0.188+0.037i -0.
106-0.159i 0.384-0.257i]
```

Fig.6: Template-Based Circuit Optimization – DD Approximation Circuit on QQCS.

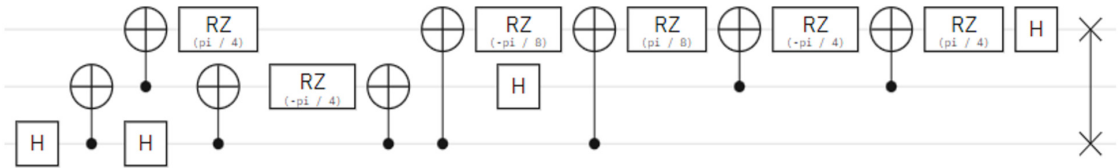


Fig.7: Linear Reversible Circuit Synthesis – DD Approximation Circuit.

tifies the essential subcircuits replacing the repetitive and common ones, providing small runtime implementation and reduced gates and levels. A method of template identification is used in [6] together with two algorithms, one for cost reduction and another for level compaction. Using a chosen quantum library, they were able to derive a quantum NCV template that is further used with the algorithm to achieve a less costly and compact circuit and attain faster synthesizing time.

Another optimization technique, introduced by Nash *et al.* [8], is presented in their paper on synthesizing linear reversible circuits using CNOT gates. The algorithm optimizes circuit size and efficiency, achieving an optimal worst-case bound regardless of connectivity constraints. This optimization is particularly beneficial for quantum systems with limited connectivity, as it effectively reduces errors and improves circuit optimization. The critical improvement of the algorithm lies in grouping multiple row operations, which proves highly effective, especially when dealing with sparse connectivity. While the al-

gorithm would benefit from further clarification and visual aids to enhance understanding, it shows great potential for practical applications in quantum computing. It can significantly contribute to quantum simulation, error correction, and optimization tasks.

These optimization techniques, employing templates and improved algorithms, highlight the ongoing efforts to enhance the efficiency and effectiveness of quantum circuits. By reducing gate and level counts, these techniques contribute to smaller runtimes and improved overall performance. Moreover, addressing limited connectivity and optimizing circuit size is crucial for advancing quantum systems.

3. HYBRID APPROACHES

The researchers laid out different hybrid approaches integrating decision diagrams and property exploitation in this section. These approaches were implemented in a 3- 3-qubit QFT circuit to investigate their efficiency in circuit simulation.

```
[ 4] |000>: __H__: __Rz(.25): _C10_: _Rz(-.25): _C10_: _Rz(.25): _H__: __Rz(.125): C20: Rz(-.125)
)__: C20: Rz(.125): __Rz(.25): _C10_: _Rz(-.25): __C10_: _Rz(.25): __H__: Sw02: M3
M1={000:0.125, 001:0.125, 010:0.125, 011:0.125, 100:0.125, 101:0.125, 110:0.125,
111:0.125}
[1 0 0 0 0 0 0] __H __Rz(0.25) _C10_ _Rz(-0.25) _C10_ _Rz(0.25) _H_ __Rz(0.125)
C20 Rz(-0.125) __C20 Rz(0.125) __Rz(0.25) _C10_ _Rz(-0.25) __C10_ _Rz(0.25) __H__ Sw
02 [0.196-0.294i 0.196-0.294i 0.196-0.294i 0.196-0.294i 0.196-0.294i 0.196-0.294i 0
.196-0.294i 0.196-0.294i]
```

Fig.8: Linear Reversible Circuit Synthesis – DD Approximation Circuit on QQCS.

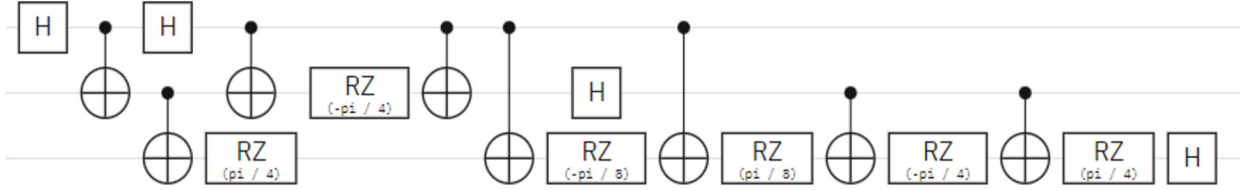


Fig.9: Reorder Trick - Template-Based Circuit Optimization – DD Approximation Circuit.

```
[ 5] |000>: H__: C01_: _C01_: H__: C01_: _Rz(-.25): _C01_: __Rz(.25): _H_: C02: __Rz(-.125): C02
: __Rz(.125): _C01_: __Rz(-.25): _C01_: __Rz(.25): __H
[1 0 0 0 0 0 0] H__ C01_ _C01_ H__ C01_ _Rz(-0.25) _C01_ __Rz(0.25) _H_ C02 __Rz(
-0.125) C02 __Rz(0.125) _C01_ __Rz(-0.25) _C01_ __Rz(0.25) __H [0.5 0 -0.354i 0.354 -
0.462i 0.191 -0.191 -0.462i]
```

Fig.10: Reorder Trick - Template-Based Circuit Optimization – DD Approximation Circuit on QQCS.

3.1 Circuit Setup

This study aimed to test a 3-qubit Quantum Fourier Transform (QFT) circuit consisting of a series of Hadamard, controlled, and SWAP gates. The researchers utilized Quick Quantum Circuit Simulation (QQCS) [2] as a computational tool to obtain the final quantum measurement of the circuit. QQCS operates by taking the linear sequence of gates in the circuit as input, starting with an initial state of $|000\rangle$, then applying the gates, and concluding with a final measurement.

This study mainly focused on optimizing a specific quantum Fourier transform (QFT) circuit, shown in Fig. 1. The QFT circuit comprised three qubits, denoted as “qubit 0,” “qubit 1,” and “qubit 2,” each represented by a separate line. It is worth noting that throughout the study, “qubit 0” was positioned on the uppermost line, “qubit 2” on the lowermost line, and “qubit 1” on the middle line. Moreover, the initial state of all qubits in the circuit was assumed to be $|0\rangle$. Thus, all the circuits in this study have an initial state of $|000\rangle$.

Fig. 2 provides the circuit sequenc in Fig. 1 and the measurement result. The simulation result includes the circuit’s initial state, followed by the gate sequence, and concludes with the measurement and probability of each final quantum state.

Although QQCS solely provides the measurement of the quantum circuit, the researchers also provided OPENQASM code for each circuit in the study. Re-

searchers employ this code to visualize and simulate the circuit in IBM Quantum Composer. The simulation in IBM Quantum Composer is a basis for the researchers to evaluate the circuit’s simulation time.

```
1 OPENQASM 2.0;
2 include "qelib1.inc";
3 qreg q[3];
4 creg meas[3];
5 h q[2];
6 cx q[2], q[1];
7 cx q[1], q[0];
8 h q[2];
9 rz(pi/4) q[2];
10 cx q[2], q[1];
11 rz(-pi/4) q[1];
12 cx q[2], q[1];
13 rz(pi/4) q[1];
14 h q[1];
15 rz(pi/8) q[2];
16 cx q[2], q[0];
17 rz(-pi/8) q[0];
18 cx q[2], q[0];
19 rz(pi/8) q[0];
20 Rz(pi/4) q[1];
21 cx q[1], q[0];
22 rz(-pi/4) q[0];
23 cx q[1], q[0];
24 rz(pi/4) q[0];
25 h q[0];
26 swap q[0], q[2];
27 barrier q[0], q[1], q[2];
28 measure q[0] -> meas[0];
29 measure q[1] -> meas[1];
30 measure q[2] -> meas[2];
```

Listing 1: OPEN QASM Code of QFT Circuit.

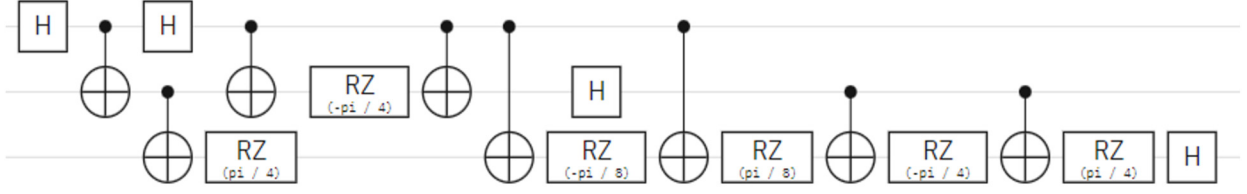


Fig.11: Reorder Trick - Linear Reversible Circuit Synthesis – DD Approximation Circuit.

```
[ 5] |000>:H__:C01_:C01:H__:C01_:Rz(-.25):C01_:Rz(.25):_H_:C02_:Rz(-.125):C02:
:_Rz(.125):C01_:Rz(-.25):C01_:Rz(.25):_H
[1 0 0 0 0 0 0] H__ C01_ C01 H__ C01_ Rz(-0.25) C01_ Rz(0.25) _H_ C02 _Rz(
-0.125) C02 _Rz(0.125) _C01 _Rz(-0.25) _C01 _Rz(0.25) _H [0.5 0 -0.354i 0.354 -
0.462i 0.191 -0.191 -0.462i]
```

Fig.12: Reorder Trick - Linear Reversible Circuit Synthesis – DD Approximation Circuit on QQCS.

Once the researchers established the experimental setup, they optimized the circuit in Fig. 1 using the approaches described in the subsequent sections of the paper.

3.2 DD Approximations

Once the researchers established the experimental setup, they optimized the circuit in Fig. 1 using the approaches. The study developed hybrid approaches that utilized the decision-diagram (DD) approximations technique alongside other methods. This technique aimed to reduce the diagram's size, enabling faster simulation while preserving the accuracy of the circuit. This approximation principle leverages the structure and properties of quantum circuits to approximate the decision diagrams, thereby reducing computational complexity and memory requirements. Consequently, simulations can be performed more efficiently without significantly sacrificing accuracy. The study employed two types of approximations: memory-driven and fidelity-driven [3].

The decision diagram nodes rely on the gates present in the circuit. Each gate type contributes a certain number of nodes to the diagram. In the context of the circuit in Fig. 1, Hadamard (H) gates create two nodes, controlled-NOT (CNOT) gates create four nodes (two for each control and target qubits), T and Rz gates create one node each, and SWAP gates create two nodes for each qubit involved [1]. Counting the gates in the circuit reveals that the original circuit in Fig. 1 has 53 nodes.

To achieve the memory-driven approximation, the researchers focused on minimizing the number of gates in the circuit, effectively reducing the overall node count. Integrating various approaches outlined in the remaining sections of the paper accomplished this approximation.

After achieving the memory-driven approximation, researchers compared the fidelity of the circuits by

evaluating their similarity to the desired target state represented in the original circuit. Fidelity served as a metric to assess the accuracy of the circuit. A high-fidelity value of 1 indicated a close resemblance between the two circuits.

In contrast, a low fidelity value, closer to 0, indicated a deviation from the desired target state. In such cases, researchers needed to make further adjustments or optimizations. Calculating the fidelity involved using the equation: $\text{fidelity} = |\langle \Psi_{\text{target}} | \Psi_{\text{circuit}} \rangle|^2$, where Ψ_{target} defined the measurement outcome depicted in the original circuit, and Ψ_{circuit} represented the measurement outcome of the circuit after applying the approaches presented in the paper.

The subsequent sections of this study presented the hybrid approaches.

3.3 Reorder Trick-DD Approximations

The QFT circuit traditionally includes SWAP gates at the end. However, this gate can lead to longer simulation times, reducing overall efficiency. To address this issue, the researchers used the reorder trick to modify the circuit in [original circuit] by swapping the gates of qubit 0 and qubit 2, eliminating the SWAP gate [7]. This manual exchange of gates improved the circuit's efficiency, as shown in Fig. 3.

Achieving memory-driven approximation, applying the reorder trick to the original circuit reduced the number of nodes from 53 to 49.

To assess the accuracy of this trick, the researchers compared the fidelity of the reordered circuit, given the measurements in Fig. 4, with the original circuit.

3.4 Template-Based Circuit Optimization-DD Approximations

Aside from the Reorder trick, quantum templates are also helpful in optimizing and synthesizing quantum circuits. Identifying a specific template to re-

```

1  OPENQASM 2.0;
2  include "qelib1.inc";
3  qreg q[3];
4  creg meas[3];
5  h q[0];
6  cx q[0], q[1];
7  cx q[1], q[2];
8  h q[0];
9  rz(pi/4) q[0];
10 cx q[0], q[1];
11 rz(-pi/4) q[1];
12 cx q[0], q[1];
13 rz(pi/4) q[1];
14 h q[1];
15 rz(pi/8) q[0];
16 cx q[0], q[2];
17 rz(-pi/8) q[2];
18 cx q[0], q[2];
19 rz(pi/8) q[2];
20 rz(pi/4) q[1];
21 cx q[1], q[2];
22 rz(-pi/4) q[2];
23 cx q[1], q[2];
24 rz(pi/4) q[2];
25 h q[2];
26 barrier q[0], q[1], q[2];
27 measure q[0] -> meas[0];
28 measure q[1] -> meas[1];
29 measure q[2] -> meas[2];

```

Listing 2: OPEN QASM Code of Reorder Trick – DD Approximation Circuit.

place $\text{rz}(\pi/8) q[2]$ in the circuit in Fig. 1, the researchers then identified additional templates using template identification in [6]. This process follows two different rules called gate-inverse rules and moving rules. Three-phase gates were eliminated using the identified template and the rules applied, further simplifying the original circuit. Figure 5 depicts the resulting circuit.

The optimization of the original circuit resulted in a decrease in the number of nodes from 53 to 50 nodes, indicating a memory-driven approximation.

Following the attainment of the memory-driven approximation, the researchers proceeded to evaluate the accuracy of the circuit by measuring the fidelity of the original circuit's measurements and the optimized circuit's measurements depicted in Fig. 6.

3.5 Linear Reversible Circuit Synthesis - DD Approximations

Gate reduction is a technique for optimizing quantum circuits, and one practical approach to achieving this is linear reversible circuit synthesis. Quantum Fourier Transform (QFT) circuits often contain multiple CNOT gates that introduce noise and are susceptible to errors. This approach focuses on minimizing the number of CNOT gates while preserving the integrity of the remaining qubit gates.

The researchers analyzed the connectivity between qubits involved in the CNOT gates to optimize the circuit. By identifying the CNOT gates that have no impact on the overall circuit, they were able to elim-

```

1  OPENQASM 2.0;
2  include "qelib1.inc";
3  qreg q[3];
4  creg meas[3];
5  h q[2];
6  cx q[2], q[1];
7  cx q[1], q[0];
8  h q[2];
9  cx q[2], q[1];
10 rz(-pi/4) q[1];
11 cx q[2], q[1];
12 rz(pi/4) q[0];
13 h q[1];
14 cx q[2], q[0];
15 rz(-pi/8) q[0];
16 cx q[2], q[0];
17 rz(pi/8) q[0];
18 cx q[1], q[0];
19 rz(-pi/4) q[0];
20 cx q[1], q[0];
21 rz(pi/4) q[0];
22 h q[0];
23 swap q[0], q[2];
24 barrier q[0], q[1], q[2];
25 measure q[0] -> meas[0];
26 measure q[1] -> meas[1];
27 measure q[2] -> meas[2];

```

Listing 3: OPEN QASM Code of Reorder Trick – DD Approximation Circuit.

```

1  OPENQASM 2.0;
2  include "qelib1.inc";
3  qreg q[3];
4  creg meas[3];
5  h q[2];
6  rz(pi/4) q[2];
7  cx q[2], q[1];
8  rz(-pi/4) q[1];
9  cx q[2], q[1];
10 rz(pi/4) q[1];
11 h q[1];
12 rz(pi/8) q[2];
13 cx q[2], q[0];
14 rz(-pi/8) q[0];
15 cx q[2], q[0];
16 rz(pi/8) q[0];
17 rz(pi/4) q[1];
18 cx q[1], q[0];
19 rz(-pi/4) q[0];
20 cx q[1], q[0];
21 rz(pi/4) q[0];
22 h q[0];
23 swap q[0], q[2];
24 barrier q[0], q[1], q[2];
25 measure q[0] -> meas[0];
26 measure q[1] -> meas[1];
27 measure q[2] -> meas[2];

```

Listing 4: OPEN QASM Code of Linear Reversible Circuit Synthesis – DD Approximation Circuit.

Table 1: Circuit Simulation Results.

		Original	Hybrid Approaches				
			Reorder Trick - DD approx	Template-Based - DD approx	Linear Reversible Synthesis - DD approx	Reorder Trick - Template-Based - DD approx	Reorder Trick - Linear Reversible Synthesis - DD approx
Quantum States	000	0.278-0.416i	0.278-0.416i	0.5	0.196-0.294i	0.5	0.196-0.294i
	001	0	0	0	0.196-0.294i	0	0.196-0.294i
	010	-0.069-0.347i	-0.069-0.347i	-0.354i	0.196-0.294i	-0.354i	0.196-0.294i
	011	0.347-0.069i	0.347-0.069i	0.354	0.196-0.294i	0.354	0.196-0.294i
	100	0.09-0.453i	0.09-0.453i	-0.462i	0.196-0.294i	-0.462i	0.196-0.294i
	101	0.188+0.037i	0.188+0.037i	0.191	0.196-0.294i	0.191	0.196-0.294i
	110	-0.106-0.159i	-0.106-0.159i	-0.191	0.196-0.294i	-0.191	0.196-0.294i
	111	0.384-0.257i	0.384-0.257i	-0.462i	0.196-0.294i	-0.462i	0.196-0.294i
Number of nodes		53	45	46	41	46	39
Simulation Time		0.0513s	0.0458s	0.0406s	0.0325s	0.0329s	0.0320s
Fidelity			1	0.59	0.5	0.59	0.5

```

1  OPENQASM 2.0;
2  include "qelib1.inc";
3  qreg q[3];
4  creg meas[3];
5  h q[0];
6  cx q[0], q[1];
7  cx q[1], q[2];
8  h q[0];
9  cx q[0], q[1];
10 rz(-pi / 4) q[1];
11 cx q[0], q[1];
12 rz(pi / 4) q[2];
13 h q[1];
14 cx q[0], q[2];
15 rz(-pi / 8) q[2];
16 cx q[0], q[2];
17 rz(pi / 8) q[2];
18 cx q[1], q[2];
19 rz(-pi / 4) q[2];
20 cx q[1], q[2];
21 rz(pi / 4) q[2];
22 h q[2];
23 barrier q[0], q[1], q[2];
24 measure q[0] -> meas[0];
25 measure q[1] -> meas[1];
26 measure q[2] -> meas[2];

```

Listing 5: OPEN QASM Code of Reorder Trick - Template-Based Circuit Optimization - DD Approximation Circuit.

```

1  OPENQASM 2.0;
2  include "qelib1.inc";
3  qreg q[3];
4  creg meas[3];
5  h q[2];
6  rz(pi/4) q[0];
7  rz(-pi/4) q[1];
8  rz(pi/4) q[1];
9  h q[1];
10 cx q[2], q[1];
11 rz(pi/8) q[0];
12 cx q[2], q[0];
13 rz(-pi/8) q[2];
14 cx q[2], q[0];
15 rz(pi/8) q[2];
16 cx q[2], q[0];
17 rz(pi/4) q[1];
18 cx q[1], q[0];
19 rz(-pi/4) q[2];
20 cx q[1], q[2];
21 rz(pi/4) q[2];
22 h q[2];
23 barrier q[0], q[1], q[2];
24 measure q[0] -> meas[0];
25 measure q[1] -> meas[1];
26 measure q[2] -> meas[2];

```

Listing 6: OPEN QASM Code of Reorder trick - Linear reversible circuit synthesis - DD approximation circuit.

inate them. The reduction in the number of gates is evident in Fig. 7, resulting in a decrease in the number of nodes and enabling faster simulations. Applying Linear Reversible Circuit Synthesis to the initial circuit allowed the generation of optimized circuits with fewer nodes, specifically decreasing from 53 to 43 nodes. Achieving this reduction was through a memory-driven approximation approach.

Following the node reduction by generating circuits with fewer gates, the researchers assessed the optimized circuit's accuracy. They compared the fidelity between the quantum states of the optimized

circuit, as depicted in Fig. 8, and the quantum state of the original circuit. This fidelity measurement served as an evaluation metric to determine the effectiveness of the optimization process.

3.6 Reorder Trick - Template-Based Circuit Optimization - and DD Approximations

Templated-based circuit optimization and the reorder trick offer avenues for further circuit optimization. This optimization can be done initially by applying the reorder trick to the circuit in Fig. 1,

yielding the circuit in Fig. 3. Following this analysis, the researchers identify a template to apply to $\text{rz}(\pi/8) \text{ q}[0]$ in the circuit. In the same manner as the templated-based circuit optimization, further templates use the two rules in [6], eliminating three-phase gates and simplifying the circuit.

After the optimization depicted in Fig. 9, through the application of Reorder Trick and Template-based Circuit Optimization, the number of nodes in the circuit was reduced from 53 to 46 nodes, resulting in a memory-driven approximation.

Subsequently, the researchers performed an accuracy assessment by measuring the fidelity between the quantum states of the optimized circuit depicted in Fig. 10 and the original circuit.

3.7 Reorder Trick - Linear Reversible Circuit Synthesis - DD Approximations

In addition to reorder trick-template-based circuit optimization, the researchers employed the linear reversible circuit synthesis technique and the reorder trick to optimize the circuit shown in the "original circuit." Initially, the reorder trick was applied to rearrange the original circuit, resulting in a reordered circuit displayed in Fig. 3. Utilizing the linear reversible circuit synthesis method, researchers eliminate unnecessary CNOT gates, leading to further optimization. This process yielded a new optimized circuit, depicted in Fig. 11.

Designing all the proposed hybrid approaches aims to minimize computational overhead while ensuring the precise simulation of quantum circuits. The main goal of these approaches is to improve the simulation of Quantum Fourier Transform (QFT) circuits by reducing both the simulation time and the amount of memory required. This reduction in computational complexity enables the simulation of larger QFT circuits, ultimately enhancing the scalability of the simulation process.

The approaches employed aim to increase the efficiency of simulating QFT circuits. They utilize optimized circuit templates to simplify the structure of the circuit, eliminating unnecessary operations and resulting in faster and more efficient simulations. Moreover, linear reversible circuits are preferred because they are easier to analyze and simulate, offering a more straightforward structure for handling the complexity of larger circuits during simulations. Collectively, these approaches focus on improving efficiency, reducing computational complexity, and enhancing scalability when simulating QFT circuits.

4. RESULTS AND DISCUSSION

The paper focused on investigating the efficiency of the proposed hybrid approaches in circuit simulation. The researchers compared the speed and accuracy of the simulations performed on circuits derived from

the original circuit. Table 1 presents the collected data from these simulations.

Table 1 provides measurements of the final state amplitudes for each circuit examined in this study. Based on these measurements, the researchers calculated the fidelity of each circuit produced by the hybrid approaches with the original circuit. The results demonstrated that all hybrid approaches closely resemble the original circuit. Notably, the reorder trick exhibited a fidelity value of 1, indicating a high similarity between the reordered and original circuits. Achieving this high fidelity was possible through the optimization performed by the reorder trick.

Manually swapping the gates kept the circuit computation unchanged. Furthermore, the hybrid approaches utilizing template-based circuit optimization and linear reversible circuit synthesis also demonstrated promising fidelity values, implying a close resemblance even after reducing the number of gates.

In terms of simulation speed, as shown in Table 1, the number of nodes directly influenced the simulation time of the circuits. The original circuit, with the highest number of nodes (53), had the longest simulation time. Conversely, the reorder trick-linear reversible circuit synthesis-DD approximation circuit, with the fewest number of nodes (39), exhibited the shortest simulation time. The impact of node count on simulation time is also observable within the circuits, with Fig. 1 having more gates than Fig. 11.

The Listings presented in this paper contain the OPENQASM code of each circuit. Observing these codes reveals that the code became shorter as the circuit was optimized. A more straightforward code indicates fewer quantum gates, therefore providing faster simulation. However, it is worth noting that the more straightforward the code, the quicker the simulation, and the circuit's quantum gates directly affect the simulation time.

Based on the presented results, the researchers observed that all hybrid approaches yielded efficient simulations. However, the Reorder Trick - Template-Based Circuit Optimization - DD approximation hybrid approach displayed the most promising results among the other hybrid approaches.

5. CONCLUSION

The researchers introduced different hybrid approaches to simplifying and optimizing quantum circuits. These hybrid approaches integrated two approaches from decision diagrams and another two from property exploitation.

The application of the hybrid approaches is presented and provides circuit optimization and simplification. The original circuit and optimized circuits were measured using Quick Quantum Circuit Simulation (QQCS) and IBM Quantum Composer to obtain simulation time.

In the test, the performance of the approaches yielded different results and was compared based on the accuracy and speed of the optimized quantum circuits.

While the study introduces hybrid approaches for circuit simplification and optimization, it does have some limitations. The study focuses primarily on a 3-qubit Quantum Fourier Transform (QFT) circuit, which may limit its applicability to larger circuits. Additionally, relying heavily on specific simulation tools may not accurately represent the performance of real quantum hardware. The evaluation primarily emphasizes accuracy and speed, potentially overlooking scalability and adaptability. The need for industry-standard benchmarks further restricts a broader assessment. Furthermore, it is essential to clarify the differences between simulations and real hardware to assess the practical effectiveness of these approaches. Finally, generalizing these approaches to other circuits remains to be determined.

6. RECOMMENDATION

The researcher highly recommends that future studies integrate the hybrid approaches presented in this study for specific purposes or functions to enrich the comprehension of their efficiency. Additionally, researchers are encouraged to investigate the impact of the placement and order of quantum gates on the accuracy of the circuit simulations. Exploring such factors can yield valuable insights into potential enhancements and advancements within the research domain. The investigation regarding the placement and order of qubit gates in the accuracy of circuit simulations could shed light on how the arrangement of gates influences the precision and reliability of quantum circuit simulations, offering vital knowledge for optimizing quantum computations and advancing the field.

ACKNOWLEDGEMENT

The completion of this research paper would not have been possible without the support and assistance of numerous individuals and organizations. The researchers would like to express deep gratitude to the Almighty God, their family, and friends for their unwavering support and encouragement throughout the research journey. They extend heartfelt appreciation to the developers of QQCS, IBM Composer, Quirk, and Munich Quantum Toolkit for providing the essential tools that enabled them to conduct simulations and experiments. Special thanks are due to Engr. Orland Tubola and Engr. Remedio Ado for their invaluable mentorship and guidance. The researchers are thankful to all those who have directly or indirectly contributed to the completion of this research paper. Their support and contributions have been truly invaluable.

AUTHOR CONTRIBUTIONS

Conceptualization, T. M. Malimban, K. R. Oropesa and O. Tubola; methodology, T. M. Malimban and K. R. Oropesa; validation, T. M. Malimban, K. R. Oropesa, C. Geron, J. K. Comia; formal analysis, T. M. Malimban and K. R. Oropesa; investigation, T. M. Malimban and K. R. Oropesa; data curation, T. M. Malimban and K. R. Oropesa; writing—draft, review and editing, T. M. Malimban and K. R. Oropesa; visualization, T. M. Malimban and K. R. Oropesa; supervision, O. Tubola and R. Ado; funding acquisition, T. M. Malimban, K. R. Oropesa, J. K. Comia and O. Tubola. All authors have read and agreed to the published version of the manuscript.

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Jade Kristine Comia was born on July 20, 2001, in the vibrant city of Calapan. From my early years, academic excellence became a constant companion, earning me the distinction of a consistent honor student. My journey led me to pursue a degree in Computer Engineering with a focus on big data. Beyond the world of algorithms and codes, my heart finds joy in two things – singing and the companionship

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