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A Technique for Improving Noise Performance of Common-Gate Fully-Differential Front-End Amplifier

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Abstract

This paper presents a technique for improving noise performance of common-gate (CG) fully-differential front-end amplifier. The circuit employs a noise canceling circuitry, which is connected in the differential configuration with tail current. The thermal noises of input CG transistors can be fully suppressed. The proposed amplifier is designed using 0.13 μm CMOS technology under 1.5 V supply. Simulation results show noise figure (NF) of 2.8 dB. The voltage gain and bandwidth of the amplifier are 15.3 dB and 1.75 GHz, respectively. The power dissipation is 12.3 mW.

Keywords: low noise, thermal noise, common gate, noise canceling, noise figure.

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1. Introduction

The technology of data communication systems is progressing very rapidly in high bit rate for both short and medium ranges. This is mainly to reduce transmission time of very large information. In those systems, it is well recognized that the design of front-end amplifiers is the most challenging, because it plays a crucial role in dictating the whole system performance. This design involves careful optimization of a number of trade offs between input impedance matching, noise, bandwidth, gain, stability and power dissipation. In addition, it is desirable to implement front-end amplifier using CMOS technology so that high level of integration can be achieved. Front-end amplifiers find various application in the hard-disk drive system (Ranmuthu et al. 2000 and Klien et al. 1994), optical system (Baker et al. 1998 and Martinez-Castillo et al. 2004), receiver (Chen et al. 2008 and Liao et al. 2007) and tuner (Song et al. 2008 and Wang et al. 2010).

Noise is one among important issues in the design of front-end amplifier, especially under a low voltage environment due to limited signal headroom. Noise represents a lower limit to the size of electrical signal that can be amplified by a circuit without significant deterioration in signal quality. Noise also results in an upper limit to the useful gain of an amplifier, because if the gain is increased without limit, the output stage of the circuit will eventually begin to limit on the amplified noise from the input stages. In a MOSFET, channel can be treated as resistor. As a result, MOSFET exhibits thermal noise, which is usually a major noise source of most MOSFET circuitries.

Recently front-end amplifier using common gate (CG) becomes a strong candidate since common-gate amplifier provides a wideband input matching over a wide operating frequency. Unfortunately, the transconductance of the common-gate amplifier cannot arbitrarily be chosen but is set by the input impedance matching requirement, thus preventing improvements of the noise figure (NF). Several approaches have been introduced to minimize the noise figure of the CG amplifier by incorporating noise canceling circuitries into the system. Chen et al. (2008) and Liao et al. (2007) proposed a noise canceling broadband CMOS CG front-end amplifiers. The resulting circuits demonstrated low noise figure. However, single-ended structure makes the circuits sensitive to common-mode noises, which is increasingly important especially in mixed-signal applications, where supply voltages could be very noisy. Song et al. (2008) employed noise-canceling technique based on a differential current amplifier. Positive feedback was used to eliminate the correlation between the input impedance, and the transconductance of the CG input transistor. Although the transistor noise on one side of the differential pair can be eliminated, the feedback path allows the transistor noise from the other side of the pair to propagate to the output. A pseudo differential structure using noise-canceling circuitries was employed (Wang et al. 2010, Jussila et al. 2008, Chen et al. 2008, Ollikainen et al. 2009 and Zare Fatin et al. 2010). Although, their designs can successfully suppress thermal noise, the pseudo differential structure makes their systems susceptible to the common-mode noises. Bruccoleri et al. (2005) and Liu et al. (2009) proposed a fully balanced noise-canceling amplifier. In their design, a differential structure with tail current is employed to perform noise canceling, and to get rid of the

common-mode noises. Unfortunately, the noise of the CG input transistor is partially suppressed.

In this paper, a fully-differential noise-canceling front-end amplifier is presented. The circuit is developed based on a common-gate amplifier. Fully differential structure with tail current is employed to minimize common-mode noises. A technique to fully suppress the CG input transistor noise is proposed. The circuit is designed using a 0.13 μm CMOS technology and operates under 1.5 V supply. The circuit demonstrates 15.3 dB passband gain, 2.8 dB noise figure, and 1.75 GHz bandwidth.

The paper is organized as follows. First, a basic balanced noise-canceling amplifier using differential structure with tail current (Bruccoleri et al. 2005) is reviewed, and the problem associated with this structure is addressed. Then, a technique for realizing fully-differential amplifier, which improves the suppression of the CG input transistor noise, is proposed. Next, the noise figure of the proposed amplifier is analyzed and compared with the noise figure of Bruccoleri et al. (2005). Finally, the simulation results, discussions and comparisons with other recent published works are provided.

2. Noise-Canceling technique using cross coupling

2.1 Noise-canceling using cross coupling

Fig. 1 illustrates a basic balanced noise-canceling amplifier (Bruccoleri et al. 2005). The circuit consists of two common gates ($M_{1a(b)}$), and noise canceling circuitry ($M_{2a(b)} - M_{3a(b)}$) connected in the differential configuration. The input impedance matching is accomplished by setting $1/g_{m1a(b)}$ to $R_S/2$. It is noted that the noise canceling circuitry employs tail current, thus making the amplifier immune to common-mode noises.

The operation of the circuit can be explained as follows. The input signal $V_{in}/2$ (solid line) undergoes a feedforward amplification, i.e., the input signal is first amplified by the common gate ($M_{1a(b)}$), and the noise canceling circuitry ($M_{2a(b)}$–$M_{3a(b)}$). The differential output signal is then taken between nodes v_{out1} and v_{out2}. Notice that the signals at nodes v_{out1} and v_{out2} have opposite phase. As a result, the differential output signal (V_{out}) is two times larger than the signal at either node v_{out1} or v_{out2} alone. This translates to an increase in the voltage gain of the system.

In term of the channel thermal noise current

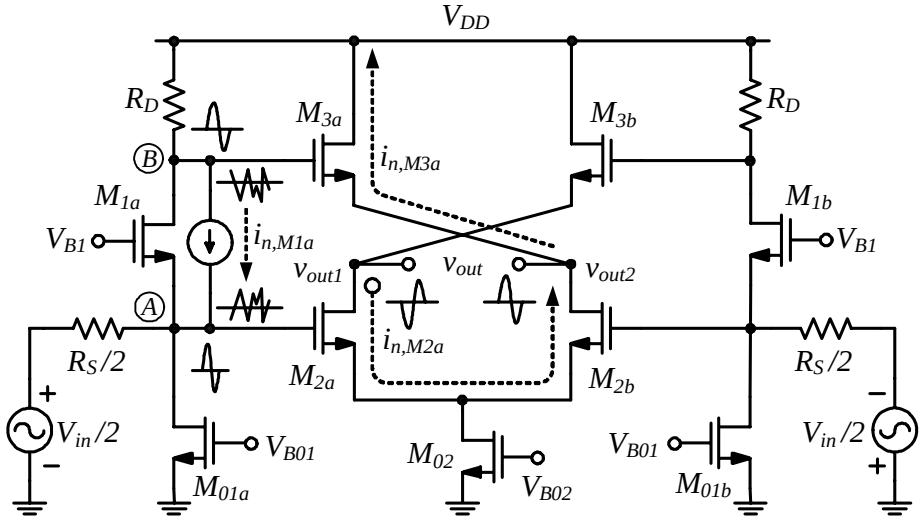

Figure 1. Balanced noise-canceling using cross coupling. (Bruccoleri et al. 2005)

(dotted signals) of a MOSFET M_{1a}, let's consider the noise current $i_{n,M1a}$ which flows into node *A* but out of node *B*. This results in two fully correlated noise voltages at nodes *A* and *B* with opposite phase. These two thermal noise voltages are further converted to currents $i_{n,M2a}$ and $i_{n,M3a}$ by M_{2a} and M_{3a}, respectively. If $i_{n,M2a}$ is equal to $i_{n,M3a}$ the output thermal noise voltage associated with M_{1a} will be completely eliminated at node v_{out2}. However, it is noticed that the thermal noise voltage at node v_{out1} still exists and could propagate to the next stage and further to the output of the system. Similarly, the thermal noise voltage of M_{1b} still exists at node v_{out2} as a result of an incomplete noise canceling as previously mentioned.

2.2 Proposed balanced noise-canceling using cross coupling

Fig. 2 illustrates the proposed amplifier, which was first proposed by Chimpleekul P. and Kasemsuwan V. (2010). As seen, the circuit is similar to the amplifier in Fig. 1. M_{4a} and M_{4b} which are connected as a common source are added at node *B*. The operation of the circuit can be explained similar to that in Fig. 1, i.e., the input signal is first amplified by the common gate ($M_{1a(b)}$) and further amplified by the noise canceling circuitry ($M_{2a(b)}$ – $M_{3a(b)}$). However, it is noticed that the common source contributes additional current to the output, thus enhancing the total gain of the system. In term of the channel thermal noise of M_{1a}, noise canceling mechanism as stated previously is still applied. However, one can see that the common source produces additional current ($i_{n,M4a}$) at output node v_{out1}. If $i_{n,M4a}$ and $i_{n,M2a}$ are set equal, the thermal noise associated with M_{1a} will now be completely eliminated at both nodes v_{out1} and v_{out2}.

The noise factor of the proposed amplifier can be analyzed and shown as

$$
\begin{aligned}
F = 1 &+ \frac{2\gamma g_{m1a(b)}\left[\left(g_{m3a(b)}+g_{m4a(b)}\right)R_D - g_{m2a(b)}R_S/2\right]^2 R_{out}^2}{R_S A_v^2} \\
&+ \frac{2\gamma g_{m2a(b)}\left(1+g_{m1a(b)}R_S/2\right)^2 R_{out}^2}{R_S A_v^2} \\
&+ \frac{2\gamma g_{m3a(b)}\left(1+g_{m1a(b)}R_S/2\right)^2 R_{out}^2}{R_S A_v^2} \\
&+ \frac{2\gamma g_{m4a(b)}\left(1+g_{m1a(b)}R_S/2\right)^2 R_{out}^2}{R_S A_v^2} \\
&+ \frac{2R_D\left(g_{m3a(b)}+g_{m4a(b)}\right)^2\left(1+g_{m1a(b)}R_S/2\right)^2 R_{out}^2}{R_S A_v^2}
\end{aligned}
\qquad (1)
$$

where γ is process dependent parameter and R_{out} is $r_{O2a(b)}//r_{O4a(b)}//(1/g_{m3a(b)})$.

From (1), the second term represents noise factor as a result of channel thermal noise

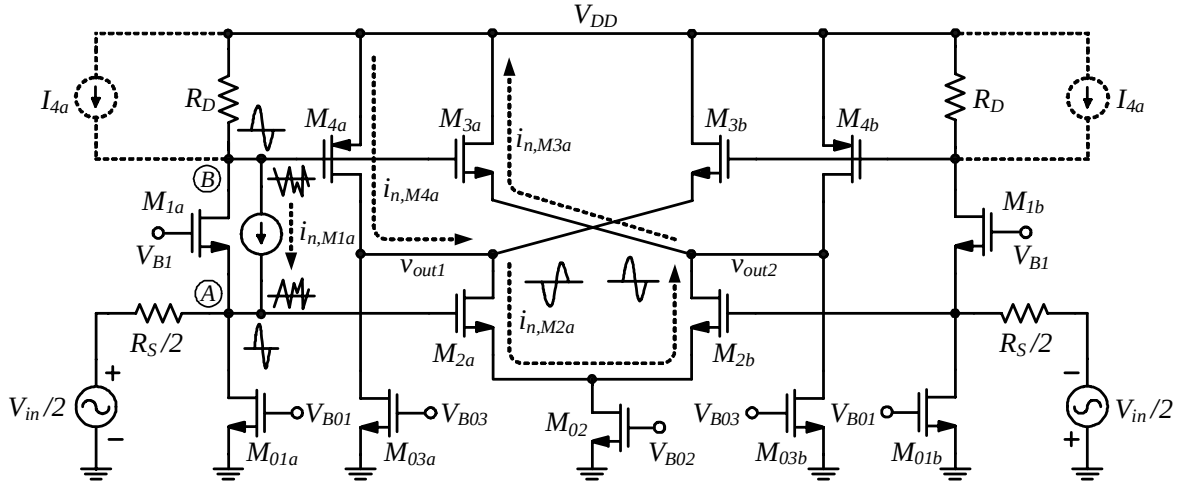

Figure 2. Proposed front-end amplifier.

associated with the common gate $M_{1a(b)}$, while the third, forth, fifth and sixth terms represents noise associated with $M_{2a(b)}$, $M_{3a(b)}$, $M_{4a(b)}$ and R_D, respectively.

One can see that if we set $(g_{m3a(b)}+g_{m4a(b)})R_D$ equal to $g_{m2a(b)}R_S/2$, the thermal noise from $M_{1a(b)}$ will be completely eliminated. It is instructive to note at this point that, the noise from the noise-canceling circuitry is also added into the system. As a result, its noise contribution to the amplifier should be addressed. In fact, the noise contribution from the noise canceling circuitry is relatively small, compared with the noise from M_{1a}. This is because the noise from the noise-canceling circuitry is divided by the gain of the common gate, when referred to the input.

The passband gain of the proposed amplifier can be analyzed using straightforward small signal analysis and shown as

$$A_v \cong \frac{\left[g_{m2a(b)} + g_{m1a(b)}\left(g_{m3a(b)} + g_{m4a(b)}\right)R_D\right]R_{out}}{\left(1+\frac{s}{\omega_{p(A)}}\right)\left(1+\frac{s}{\omega_{p(B)}}\right)\left(1+\frac{s}{\omega_{p(out)}}\right)} \quad (2)$$

Where ω_{pA}, ω_{pB}, $\omega_{p(out)}$, are poles associated with nodes *A*, *B* and output, repectively, and given by

$$\omega_{p(A)} \cong \frac{g_{m1a(b)}}{\left[\begin{array}{l} C_{gs1a(b)} + C_{sb1a(b)} + C_{gd01a(b)} + C_{db01a(b)} \\ +C_{gd2a(b)}\left(1+g_{m2a(b)}R_{out}\right) + C_{gs2a(b)} \end{array}\right]}$$

$$\omega_{p(B)} \cong \frac{1}{R_D\left[\begin{array}{l} C_{gd1a(b)} + C_{db1a(b)} + C_{gd3a(b)} + C_{gs4a(b)} \\ +C_{gd4a(b)}(1+g_{m4a(b)}R_{out}) \end{array}\right]}$$

$$\omega_{p(out)} \cong \frac{1}{R_{out}\left(\begin{array}{l} C_{gd2a(b)} + C_{db2a(b)} + C_{sb3a(b)} + C_{gd4a(b)} \\ +C_{db4a(b)} + C_{db03a(b)} + C_{gd03a(b)} \end{array}\right)}$$

Since $\omega_{p(out)} << \omega_{p(A)}$, $\omega_{p(B)}$, the circuit has one dominant pole (at node $v_{out1(2)}$) and, therefore, the bandwidth (ω_{-3dB}) of the proposed amplifier can be approximated as $\omega_{-3dB} = \omega_{p(out)}$.

One can increase the gain of the circuit in Fig. 2 by adding two current sources I_{4a} and I_{4b} (dashed line) in Fig. 2. These current sources allow larger R_D for the same common-gate bias current, resulting in larger gain. We have found that gain of the circuit can go up to 30 dB, when current sources (implemented using a simple long channel PMOS transistor) are employed. However, one should be careful with this gain enhancement technique, because this also affects the input impedance and noise figure of the system.

3. Results and discussion

To verify the circuit performance, HSPICE is used to simulate the proposed circuit, using a 0.13 μm CMOS process with 1.5V supply voltage. In this work, the bias currents are chosen to optimize voltage gain, speed, noise figure, power dissipation, and bandwidth of the circuit. The transistor dimensions of the proposed circuit are summarized in Table 3.1. In addition, the input impedance is also designed to match with the source impedance (50Ω) to ensure maximum power transfer, and minimize any reflection.

Fig. 3 shows a comparison between noise figures of the circuits in Fig. 1 (dash) and Fig. 2 (solid), which read 3.1 dB and 2.8 dB at 1 Hz, respectively. It is noted that, for a fair comparison, the same CMOS technology and transistor dimensions for both circuits are employed. As seen, the noise figure of the circuit in Fig. 2 is less than that of the circuit in Fig. 1. This is due to the common-source transistor $M_{4a(b)}$, which allows full suppression of the CG input transistors.

TABLE 3.1 Device dimensions

Device	Size (W/L) [μm/μm]
$M_{1a(b)}$	300/0.18
$M_{2a(b)}$	190/0.18
$M_{3a(b)}$	50/0.18
$M_{4a(b)}$	220/0.18
$M_{01a(b)}$	45/0.9
M_{02}	115/0.9
$M_{03a(b)}$	30/0.9
Resistor	
Device	Values [Ω]
R_D	175

Fig.4 shows frequency response of the amplifier in Fig. 1 (dash), and the proposed differential amplifier in Fig. 2 (solid). The passband gain of the proposed circuit is found to be 15.3 dB, while the bandwidth of the circuit is 1.75 GHz. Larger gain is obtained since the common-source transistor $M_{4a(b)}$ contributes additional current to the output.

Fig. 5 shows eye diagrams of the proposed amplifier at 1.4 Gb/s. The results are obtained by applying the pseudo random input to the amplifier, and subsequently superimpose the output data every 1.37 ns. The simulation shows 93.0 % and 98.2% horizontal eye opening and vertical eye opening, respectively. As seen, the eye is wide opening, indicating that the proposed amplifier can operate at high bit rate with small ISI and bit error rate.

Table 3.2 summarizes and compares the performances of our design with other recent published CMOS front-end amplifiers. As seen, the proposed differential circuit demonstrates relatively low noise figure (NF), while all other parameters are found to be comparable. It is noted that although the result from Chen et al. (2008) shows smaller noise figure, the single-ended structure was employed in their design, making the system susceptible to common mode noises. In addition, the power dissipation would be high, if their single-ended structure would have to be modified to the differential one.

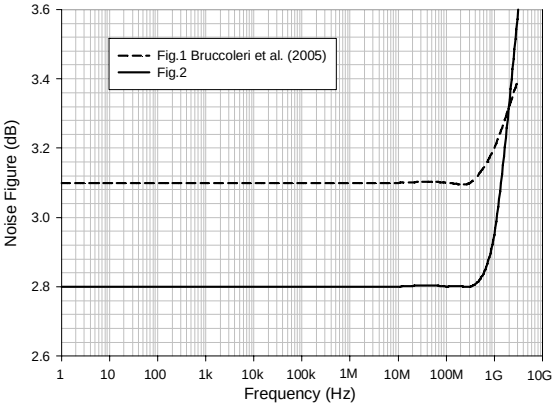

Figure 3. Noise figure.

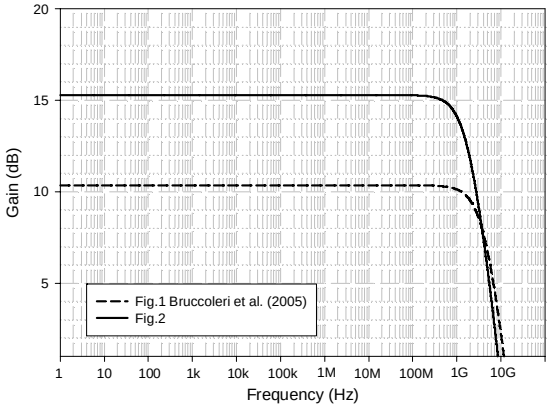

Figure 4. Frequency response.

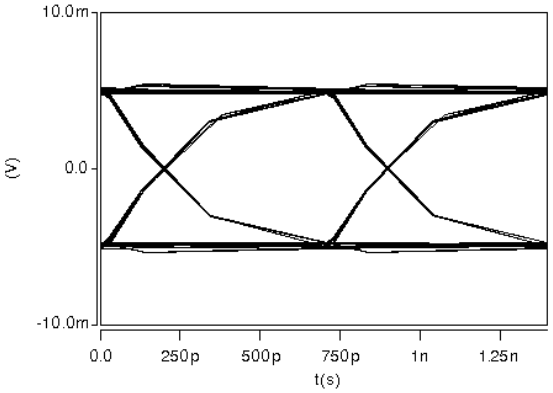

Figure 5. Eye diagram at 1.4 Gb/s.

TABLE 3.2 Performance comparison

Reference	Chen et al.	Liao et al.	Song et al.	Jussila et al.	Liu et al.	Fig.2
BW [GHz]	0.8-2.1	1.2-11.9	0.02-0.17	2.1	2.1-11.2	1.75
Gain [dB]	14.5	9.7	20.5	5.2	28.2	15.3
NF [dB]	2.6	4.5	3.3	3	3.7	2.8
Differential	No	No	Yes	Yes	Yes	Yes
Technology [μm]	0.13	0.18	0.18	0.13	0.18	0.13
Supply[V]	1.5	1.8	1.8	1.2	1.8	1.5
Power [mW]	17.4	20	18	12.6	12.5	12.3

4. Conclusion

In this paper, a differential CMOS front-end amplifier using a technique for improving noise performance of common-gate fully-differential front-end amplifier is presented. The circuit employs a noise canceling circuitry, which can fully eliminate noise from the input common-gate transistor. Noise canceling circuitry has differential structure with tail current, making the proposed circuit immune to common-mode noises. The simulation results show low noise figure, low power consumption and wide bandwidth. The proposed front-end amplifier is suitable for a first stage amplifier such as the reading part of hard disk drive systems.

5. Acknowledgment

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