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A fully differential full-wave rectifier using current conveyors *

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Abstract

This work presents a fully differential full-wave rectifier using current conveyors. Both input and output signals of the proposed rectifier can be differential or single modes. The proposed rectifier consists of two current conveyors, a positive full-wave current rectifier, a negative full-wave current rectifier and two MOS-resistors. The proposed rectifier uses all MOS structure. Simulation results from the layout in a 0.5 μm MOS technology of AMI are obtained by using the level 49 model through MOSIS. The results showing the operation of the proposed rectifier at the frequencies of 1 MHz and 100 MHz are included.

Keywords: rectifier, CMOS circuit

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Introduction

Rectifiers are extensively used in wattmeters, AC voltmeters, RF demodulators, piecewise linear function generators, and various nonlinear analog signal-processing circuits. The operation of a simple diode rectifier is limited by the threshold voltage of a diode, approximately 0.3 V for a germanium diode and 0.7 V for a silicon diode, thus the simple diode rectifier is used only in some applications in which the precision in a range of the threshold voltage is insignificant, such as radio frequency demodulators and DC voltage supply rectifiers. However, for applications requiring accuracy in the range of the threshold voltage, the simple diode rectifier cannot be used. This can be overcome by using integrated circuit (IC) rectifiers instead.

In the past, many integrated circuit full-wave rectifiers have been proposed. Most of the integrated circuit full-wave rectifiers proposed do not operate in a fully differential mode (both input and output being a single mode, or input as the differential mode but output as the single mode). In the single mode, one of two inputs has to be grounded, causing that the rectifier cannot apply to a differential input to not refer to ground. Additionally, one of two outputs must also be grounded; this results in that the rectifier cannot supply the output to a floating load or a floating input of a next circuit.

Recently, the full-wave rectifiers using current conveyors have been proposed. These full-wave rectifiers yield a main advantage in view of the high frequency operation. LTP Electronics Ltd. (1993) and Khan *et al.* (1995) originally proposed the same current conveyor full-wave rectifiers as shown in figure 1(a). This full-wave rectifier was developed to reduce the distortion due to the small-signal dV / dt limitation by Toumazou *et al.* (1994) with the addition of a DC voltage source as shown in figure 1(b). Hayatleh *et al.* (1994) further developed the full-wave rectifier to reduce the effect of temperature on the zero crossing performance by using a current source and a resistor in place of the voltage source as shown in figure 1(c). The above current conveyor full-wave rectifiers can apply to the differential input but cannot to the differential output.

In this work, the author will develop the current conveyor full-wave rectifier to be able to operate in the fully differential mode (be able to use with differential input and output). Moreover, the development yields the better points as follows.

1) Each of the above current conveyor full-wave rectifiers uses two passive resistors while the proposed full-wave rectifier uses all MOS structure. Hence, the proposed rectifier is more suitable for integrated circuit fabrication.
2) The above current conveyor full-wave rectifiers use commercial current conveyors, leading to the use of high supply voltage. The proposed rectifier uses the specially

designed current conveyors that use the lower supply voltage (±2 V), leading to lower power consumption.

3) Since current conveyors in the 0.5 μm MOS technology are used in the proposed rectifier, the operation frequency of the proposed rectifier is higher.

Proposed fully differential full-wave rectifier using current conveyors

A proposed fully differential full-wave rectifier using current conveyors is shown in figure 2, which consists of two second-generation current conveyors (CCIIs), one positive full-wave current rectifier, one negative full-wave current rectifier, and two MOS-resistors. The CMOS circuit of current conveyors [Bruun. 1993] is shown in figure 3. Each current conveyor in the proposed rectifier has four nodes, of which the relations of voltages and currents are given by

$$\left.\begin{aligned} i_Y &= 0 \\ v_X &= v_Y \\ i_{Z+} &= i_X \\ i_{Z-} &= -i_X \end{aligned}\right\} \quad (1)$$

Comparing the proposed rectifier with the above rectifiers, one finds that a resistor connected between nodes X is not used for the proposed rectifier. This is compensated by using the low current I_C in the circuit of figure 3 to increase the resistance at nodes X (R_x) of current conveyors [Bruun. 1993], normally, this resistance is very low. Another advantage of using the low current I_C is to consume low power.

Using (1) one finds that

$$i_{Z+1} = i_{Z-2} = -i_{Z-1} = -i_{Z+2} = \frac{V_{in}}{2R_x} \quad (2)$$

where $V_{in} = V_{in+} - V_{in-}$; for a single mode application, V_{in-} has to be grounded.

Currents I_{Z+1} and I_{Z-1} are fed to the positive full-wave current rectifier that comprises four MOS-diodes, MD1 to MD4, [Monpapassorn *et al.* 2001] the drain and source together connected as cathode while the substrate as anode. When I_{Z+1} is positive, I_{Z-1} is negative, I_{Z-1} flows through

MD1 as I_{O+}, I_{Z-1} is bypassed to ground by MD3. Inversely, when I_{Z+1} is negative, I_{Z-1} is positive, MD4 conducts I_{Z-1} as I_{O+}, MD2 conducts I_{Z+1} to ground. This operation leads to

$$\left.\begin{aligned} V_{in} > 0;\ I_{O+} &= \frac{V_{in}}{2R_x} \\ V_{in} < 0;\ I_{O+} &= \frac{-V_{in}}{2R_x} \end{aligned}\right\} \tag{3}$$

Therefore I_{O+} is a positive full-wave current.

The inputs of the negative full-wave current rectifier (MD5 to MD8) are I_{Z+2} and I_{Z-2} When I_{Z+2} is positive, I_{Z-2} is negative, I_{Z+2} is bypassed to ground by MD6, I_{Z-2} flows through MD8 as I_{O-}. In the opposite way, when I_{Z+2} is negative, I_{Z-2} is positive, I_{Z+2} flows through MD5 as I_{O-}, I_{Z-2} is bypassed to ground by MD7. This operation yields

$$\left.\begin{aligned} V_{in} > 0;\ I_{O-} &= \frac{-V_{in}}{2R_x} \\ V_{in} < 0;\ I_{O-} &= \frac{V_{in}}{2R_x} \end{aligned}\right\} \tag{4}$$

It is evident in (4) that I_{O-} is a negative full-wave current.

MOS-resistors [Wang. 1990], R_A and R_B, convert currents I_{O+} and I_{O-} to the positive full-wave voltage (V_{out+}) and the negative full-wave voltage (V_{out-}), respectively. The resistance of the MOS-resistor is given by

$$R = \frac{1}{2KV_{DT}} \tag{5}$$

where two NMOSs in the MOS resistor have the same characteristics; $K = \mu C_{ox} W/L$, μ is the mobility of carriers, C_{ox} is the gate capacitance per unit area, W and L are the channel width and length; $V_{DT} = V_{DD} - V_T = -(V_{SS}+V_T)$, $V_{DD} = -V_{SS}$, V_T is the threshold voltage.

If one sets the W/L ratios of NMOSs in two MOS-resistors to obtain $R = 2R_x$, exploiting (3) and (4), one can write V_{out+} as

$$\left.\begin{aligned} V_{in} > 0;\ V_{out+} &= V_{in} \\ V_{in} < 0;\ V_{out+} &= -V_{in} \end{aligned}\right\} \tag{6}$$

and V_{out-} as

$$\left.\begin{aligned} V_{in} > 0;\ V_{out-} &= -V_{in} \\ V_{in} < 0;\ V_{out-} &= V_{in} \end{aligned}\right\} \tag{7}$$

Equations, (6) and (7), show that V_{out+} and V_{out-} are a positive full-wave voltage and a negative full-wave voltage in the case of the single mode output (one output for use, another for ground). For the differential mode output, both outputs have to be together used, by using $R = R_x$, one obtains the positive full-wave rectification as

$$\left.\begin{aligned} V_{in} > 0;\ V_{out+} - V_{out-} &= V_{in} \\ V_{in} < 0;\ V_{out+} - V_{out-} &= -V_{in} \end{aligned}\right\} \tag{8}$$

and the negative full-wave rectification as

$$\left.\begin{aligned} V_{in} > 0;\ V_{out-} - V_{out+} &= -V_{in} \\ V_{in} < 0;\ V_{out-} - V_{out+} &= V_{in} \end{aligned}\right\} \tag{9}$$

which are the fully differential full-wave rectification.

Simulation results

The author will verify a proposed fully differential full-wave rectifier by using its layout in a 0.5 μm MOS technology of AMI as shown in figure 4 for simulation, the parasitic capacitance is included in simulation. The level 49 model of this technology is obtained through MOSIS, as shown in Table 1. The W/L ratios of MI1 to MI5 are based on 10 μm / 1 μm and those of M1 to M14 are based on 20 μm / 1 μm. A supply voltage used is ± 2 V. The constant current sources (I_C) of current conveyors are 20 μA. The bias voltages V_{bias+} and V_{bias-} are 0.7 V and – 0.7 V, respectively, these bias voltages make all MOS-diodes to turn-on all the time to reduce the on/off

transition problem at high frequency [Toumazou *et al.* 1994]. If the precise temperature stability is needed, the bias voltage sources[Monpapassorn *et al.* 2001] should be applied.

One feeds the sample 1 MHz and 100 MHz sine wave signals (100 mVpeak) at an input of the proposed full-wave rectifier operating in fully differential mode, then one gets the operation as shown in figure 5 and figure 6, respectively. One finds the error of an output voltage, compared with the absolute value of an input voltage, from figure 5 to be lower than 1 %, which results from carefully adjusting the W/L ratios of MOSs in MOS-resistors to compensate the effect of R_x. In figure 5, the output signal is evidently delayed from the input signal due to the effect of the equivalent capacitors of the circuit. In addition, the amplitude of the output signal decreases because of the decrement of the transferring gains of current conveyors at high frequency. The input and output delay must be considered in use and the input and output amplitude error can be compensated by adjusting the W/L ratios of MOSs of R_A and R_B to get the suitable resistance. The power consumption in this simulation from a reported file of the SPICE program is not more than 1.2 mW, which is much lower than that of the above current conveyor full-wave rectifiers.

Conclusion

In this work, the author has reported the design and simulation of a fully differential full-wave rectifier using current conveyors. The advantages of the proposed full-wave rectifier, compared with the previously proposed current conveyor full-wave rectifiers, are using lower supply voltage, consuming lower power, yielding wider operation frequency range, forming all MOS structure, and applying both single and differential modes. It should be noted on the use of the proposed rectifier that it is suitable for a high impedance load. If a low impedance load is applied, the proposed rectifier needs the buffers at outputs.

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Table 1 *Model used in simulation.*

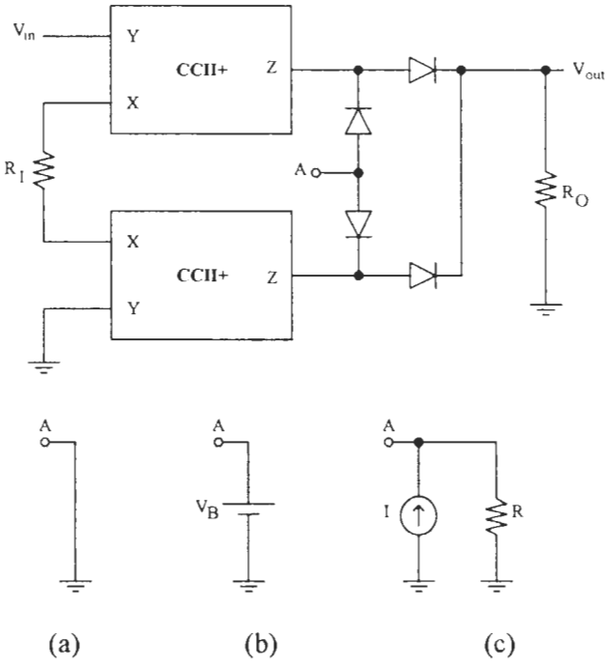


Figure 1 *Current conveyor rectifiers: (a) proposed by LTP Electronics Ltd. and Khan et al., (b) proposed by Toumazou et al., (c) proposed by Hayatleh et al..*

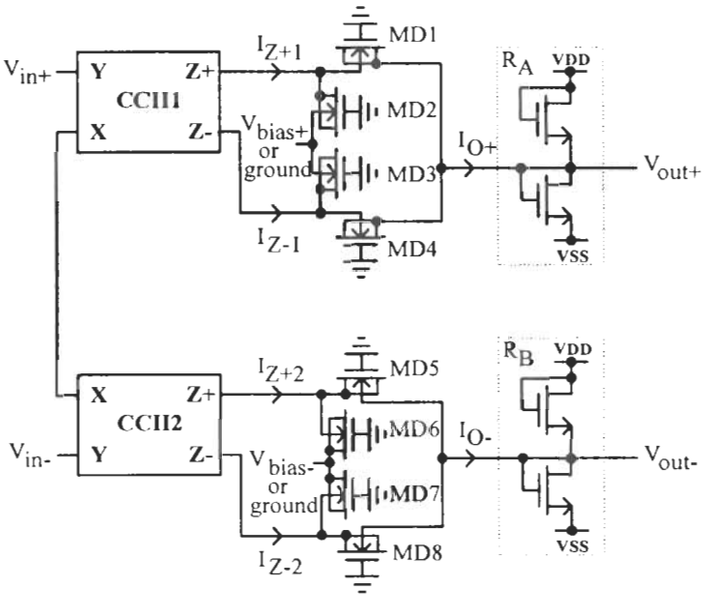


Figure 2 *Proposed fully differential full-wave rectifier.*

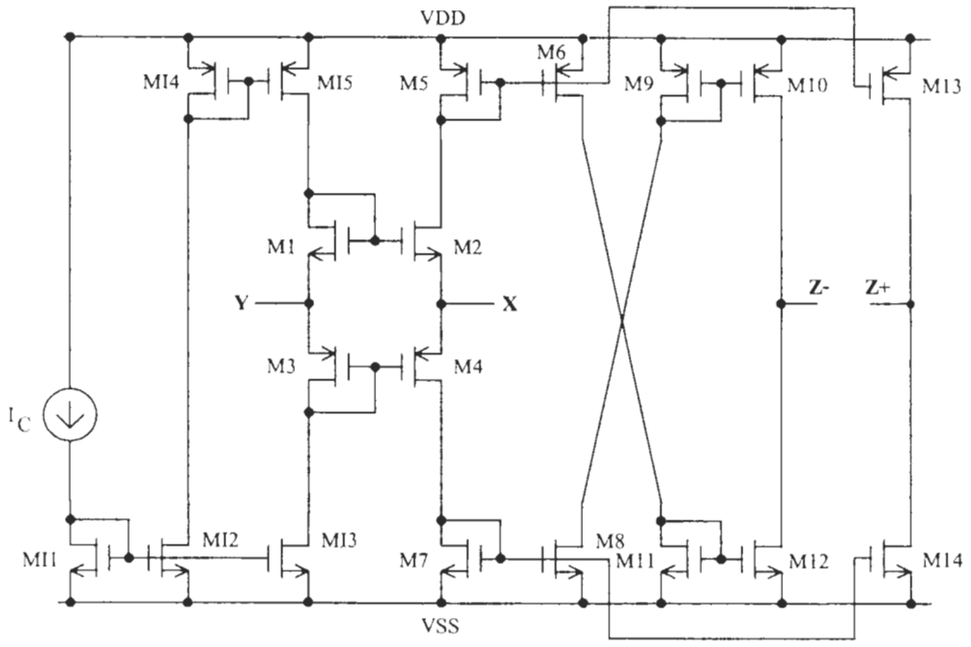


Figure 3 *Circuit of CCIIs in figure 2.*

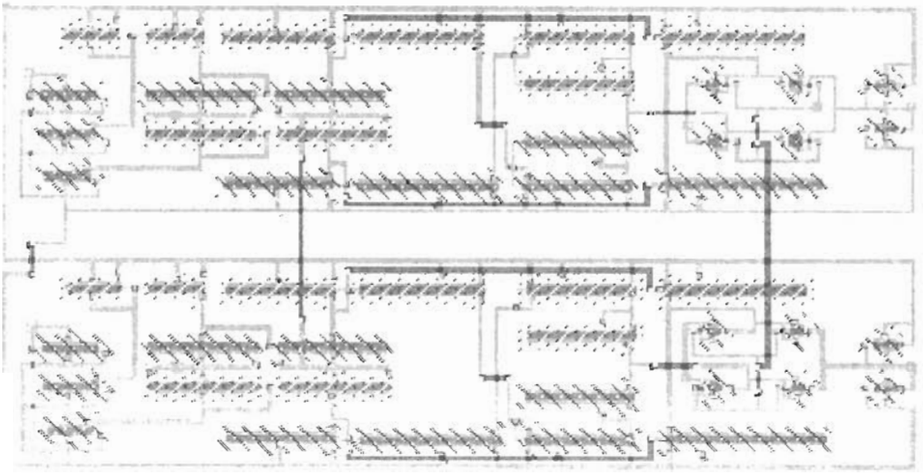
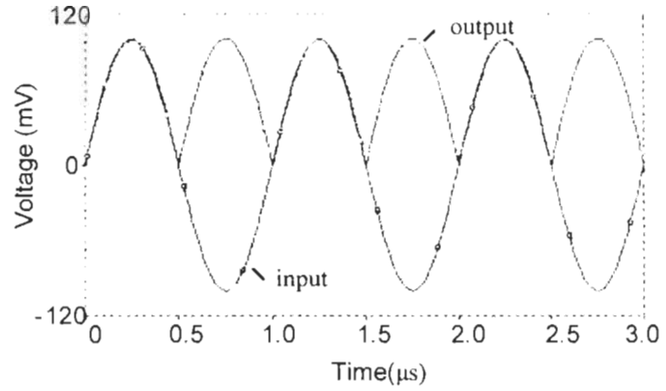
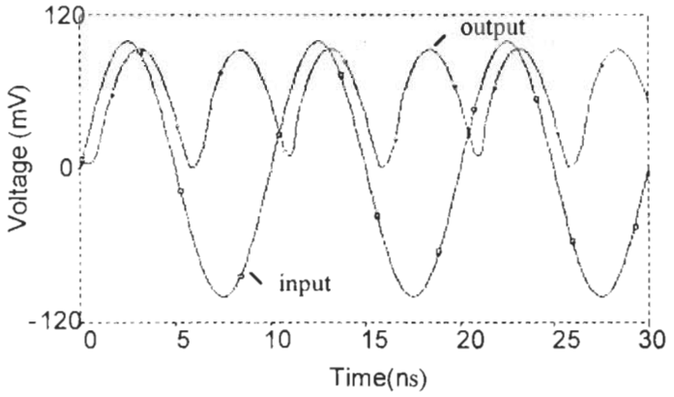


Figure 4 *Layout of the proposed fully differential full-wave rectifier.*



Amplitude error ≈ 0.9 %
Time delay ≈ 0.015 μs

Figure 5 *Operation of the proposed rectifier at the frequency of 1 MHz.*



Amplitude error ≈ 9 %
Time delay ≈ 0.8 ns

Figure 6 *Operation of the proposed rectifier at the frequency of 100 MHz.*