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วงจร CDBA แบนด์วิดกว้าง แบบใช้แรงดันไฟเลี้ยงต่ำ และ การนำไปประยุกต์ใช้ในวงจรกรองสัญญาณแลดเดอร์โหมดกระแส *

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บทคัดย่อ

บทความนี้นำเสนอการออกแบบวงจร current differencing buffered amplifier (CDBA) เพื่อการนำไปประยุกต์ใช้ในงานประมวลผลสัญญาณแบบใช้แรงดันไฟเลี้ยงต่ำ วงจร CDBA ที่นำเสนอมีรูปแบบง่ายและสามารถทำงานได้ที่แรงดันไฟเลี้ยงต่ำสุดประมาณ 2 โวลท์ สมรรถนะในการทำงานของวงจรที่ได้นำเสนอถูกแสดงด้วยผลการเลียนแบบการทำงานของวงจรด้วยโปรแกรม PSPICE นอกจากนี้ยังได้นำเสนอแนวทางการนำไปประยุกต์ในการเลียนแบบโครงสร้างแบบ leapfrog เพื่อสังเคราะห์เป็นวงจรกรองสัญญาณแลดเดอร์โหมดกระแสย่านความถี่สูงอีกด้วย

คำสำคัญ: วงจร CDBA , วงจรโหมดกระแส, วงจรกรองสัญญาณแลดเดอร์ , วงจรแรงดันไฟเลี้ยงต่ำ

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Low-Voltage Wide-Bandwidth CDBA and Its Application to Current-Mode Ladder Filters *

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Abstract

In this paper, a design of current differencing buffered amplifier (CDBA) for low-voltage applications is presented. The proposed CDBA is simple and is designed to operate with a minimum power supply of 2 volts. The PSPICE simulation results demonstrating the circuit performance are included. Some design procedures using this CDBA as an active element in the leapfrog simulation of high frequency current-mode ladder filters are also introduced.

Keywords: Current Differencing Buffered Amplifier (CDBA), current-mode circuit, ladder filter low-voltage circuit

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Introduction

During the past few years, comparing with voltage-mode techniques, current-mode signal processing techniques have been received a wide attention due to its wide bandwidth, low-voltage operation and simple implementation of signal operations such as addition and subtraction. Usually, the design of high performance current-mode circuits employ circuit building blocks such as second-generation current conveyors (CCIIs) and current feedback amplifiers (CFAs). Recently, a current differencing buffered amplifier (CDBA) has been first proposed [C. Acar and S. Ozoguz. 1999.] which is particularly suitable for the current-mode operation and realization of continuous-time filters. The CDBA can offer high-slew rate, wide bandwidth and simple implementation [S. Ozoguz. A. Toker. and C. Acar. 1999.] It is beneficial to use CDBAs as a building block to realize the most general n^{th}-order voltage-mode and current-mode transfer functions [C. Acar and H. Sedef. 2003.] In addition, CDBA-based circuit implementation is suitable for current-mode continuous-time fully integrated MOSFET-C filters, especially for filters using MOS resistive circuit, MRC [S. Ozoguz. A. Toker. and C. Acar. 1999.],[Takagi. Z.Czarnul. T.Iida. and N. Fujii. 1997]. Despite the fact that several CDBAs have been reported in the literature [C. Acar and S. Ozoguz. 1999., S. Ozoguz. A. Toker. and C. Acar. 1999.], there are no circuits that can operate at a low supply voltage. A low-voltage technique is one of the most important issues because of the advance of the large-scale integration with complicated circuit systems and the increasing demands for battery-operated portable equipments. This paper proposes a low-voltage CDBA, which can operate at a low DC power supply voltage of 2 volts. The PSPICE simulation results of the proposed low-voltage CDBA show a low power consumption and a wide bandwidth. Since the proposed circuit considerably simplifies the realization of high frequency current-mode active ladder filters, a realization of the leapfrog structure of current-mode ladder filters in which CDBA is employed as an active element is shown as an application of the CDBA. The presented method shows that the CDBA-based leapfrog simulation is simple and suitable for realizing of the current-mode ladder filters. Most importantly, the current-mode ladder filters with CDBAs employ less active components compared with CCIIs-based ladder filter implementations [E.I. El-Masry. 1996.]

Basic Principle

The representation of the CDBA is shown in Fig.1 whose current and voltage characteristics can be described by the following relations [C. Acar and S. Ozoguz. 1999 and C. Acar and H. Sedef. 2003.] :

$$v_p = 0 \quad , \quad v_n = 0 \quad , \quad i_z = i_p - i_n \quad \text{and} \quad v_w = v_z \tag{1}$$

It should be noted from the above expression that the differential input current i_p-i_n is converted to the output voltage v_w through an impedance connected at the port z. Thus the CDBA basically consists of two blocks ; a current differencing circuit (current subtractor) and a voltage follower. In the following section, we will introduce a low-voltage current differencing circuit providing the difference of the input currents i_p and i_n and a low-voltage buffered voltage amplifier.

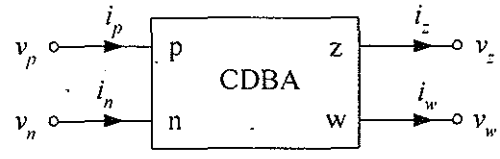


Figure 1 *Circuit representation of a CDBA*

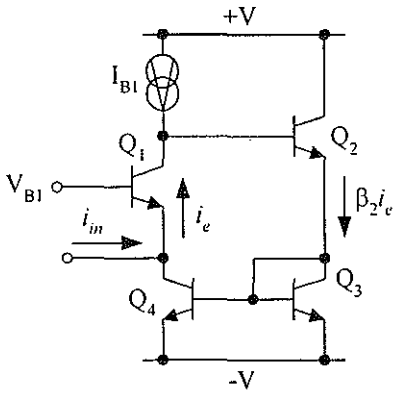


Figure 2 *Low-input resistance input stage*

Low-Input Resistance Input Stage

Fig.2 shows a low-input resistance input stage, where the transistors Q1-Q4 function as a feedback loop [T. Nagasaku. A. Hyogo. and K. Sekine. 1996.]. Assuming that the emitter signal current of Q1 is ie, the emitter current of Q2 will approximately be equal to β2ie. The current mirror formed by Q3-Q4 reflects the current β2ie to the collector current of Q4. Therefore, the input signal current iin can be expressed as ;

$$i_{in} = i_e + \beta_2 i_e \tag{2}$$

Due to the negative feedback, the input resistance r_{in} of this circuit is very low and can be given by

$$r_{in} \cong \frac{r_{e1}}{\beta_2} \tag{3}$$

where β_2 is the current gain of the transistor Q_2, r_{e1} is the small signal emitter resistance which is given by $r_{e1} = \frac{V_T}{I_{B1}}$ and V_T is the thermal voltage. Based on the low-input resistance input stage of Fig.2, in the following section a current subtractor will be developed.

Current Subtractor

The unity gain current amplifier based on the above input stage is shown in Fig.3. A biasing circuit comprising the transistor Q_6 and the bias current source I_{B2} is added to provide the bias voltage V_{B1} and the imaginative ground at the input node, while the transistor Q_5 and the bias current source I_{B3} provide the output current i_{out}. Since the relationship between the input signal current i_{in} and the signal current i_e can be given by,

$$i_e = \frac{i_{in}}{\beta_2 + 1} \tag{4}$$

thus, the output signal current i_{out} of the circuit of Fig.3 can be expressed as

$$i_{out} = -\beta_2 i_e = -\frac{\beta_2}{\beta_2 + 1} i_{in} \tag{5}$$

In general case, the current gain $\beta_2 >> 1$, thus the output current i_{out} of this circuit can be written as

$$i_{out} \cong -i_{in} \tag{6}$$

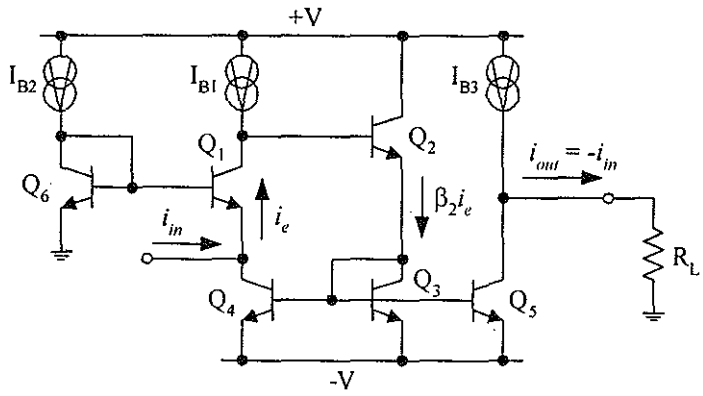


Figure 3 *Unity gain current amplifier*

Fig.4 shows the proposed current subtractor circuit, which is obtained by using two unity gain current amplifiers that are formed by Q_1-Q_5 and Q_7-Q_{11}. The current mirror Q_{12}-Q_{13} reflects the current i_p to the output port, therefore, the output current of this circuit can now be expressed as

$$i_{out} = i_p - i_n \tag{7}$$

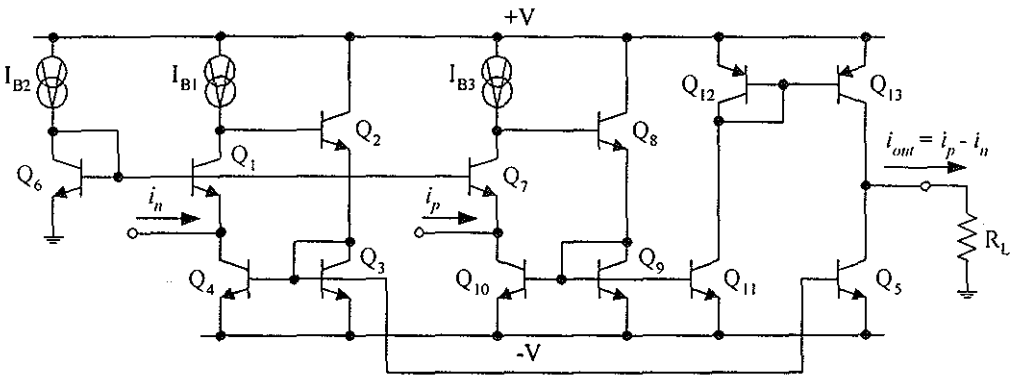


Figure 4 *Current subtractor*

Buffered Voltage Amplifier

The high-input impedance voltage amplifier based on a simple emitter follower is presented in Fig.5, where complementary NPNs and PNPs, Q_{14}-Q_{17}, form an input buffer that forces the w terminal voltage to that of the z terminal. Let us assume that all transistors are well matched and a good matching in V_{BE} between NPN and PNP transistors is obtained in order to achieve low offset voltage. Thus, the input impedance at the port z becomes very high and is approximately equal to

$$r_z \cong \beta_n \beta_p \left[\frac{r_e}{2} + R_w \right] \tag{8}$$

where $\beta_n = \beta_{14} \cong \beta_{16} >> 1$, $\beta_p = \beta_{15} \cong \beta_{17} >> 1$, $r_e = r_{e14} = r_{e16} \cong r_{e15} = r_{e17}$ and R_w is the load resistance connected to the port w. On the other hand, the output impedance at the port w becomes quite low and is equal to

$$r_w \cong \left[\frac{r_e}{2} + \frac{R_z}{\beta_n \beta_p} \right] \tag{9}$$

where R_z is a converting resistor connected to the port z. For example, if R_z = 1 kΩ, R_w = 10 kΩ, V_T = 26 mV, $I_{B4} = I_{B5}$ = 100 μA and $\beta_n \cong \beta_p$ = 100, then r_z and r_w are approximately equal to 10 MΩ and 130 Ω, respectively.

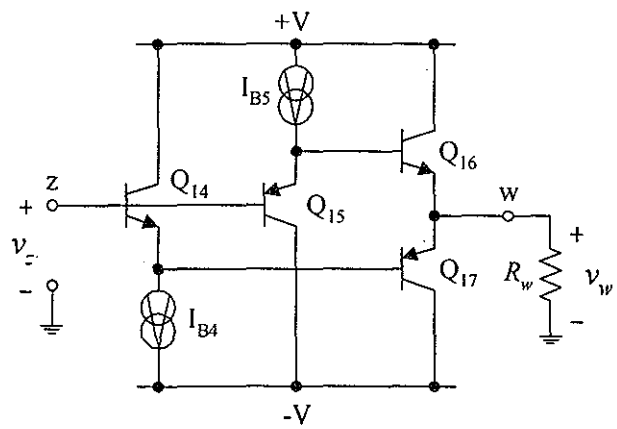


Figure 5 *Buffered voltage amplifier*

Low-Voltage Current Differencing Buffered Amplifier (CDBA)

The proposed low-voltage CDBA is now shown in Fig.6, which consists of a current subtractor of Fig.4 and a buffered voltage amplifier of Fig.5. All bias current sources of the circuit are realized by current mirror circuits and set to be equal to I_B. Since the circuit uses only two transistors and one bias current source between the positive and the negative supply voltages, this circuit can operate at a low power supply voltage of 2 volts (or ±1 volts).

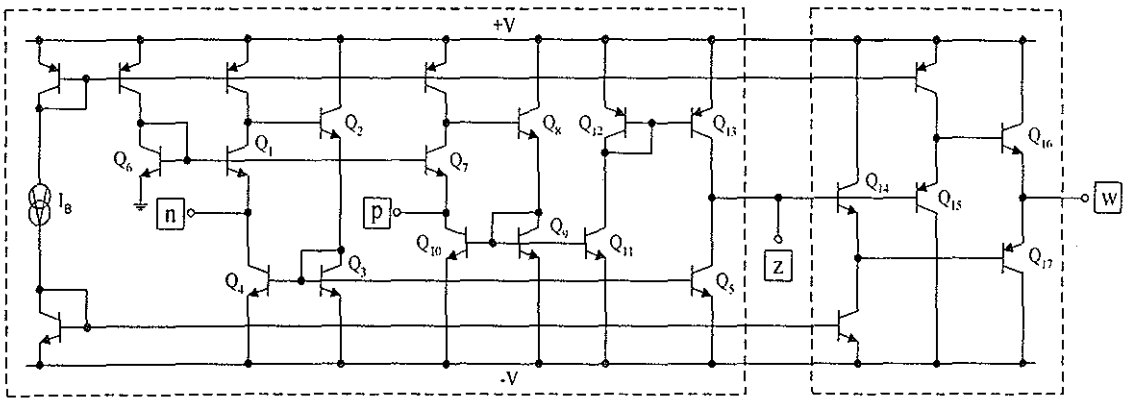


Figure 6 *Circuit diagram of the proposed low-voltage CDBA*

Circuit Performance Analysis

By using a hybrid-π model and a routine small-signal circuit analysis, the performance of the proposed low-voltage CDBA of Fig.6 can be analyzed as follows. Since the differential input current i_p-i_n is converted to the output voltage v_w through the resistance R_z which is connected at the port z, thus the relationship between the input and output signals of this device can be described in the term of the trans-resistance gain R_m as

$$\frac{v_w}{i_p - i_n} = R_m = R_z\left(\frac{1}{1+\varepsilon_i}\right)\left(\frac{1}{1+\varepsilon_v}\right) \tag{10}$$

where ε_i is the current transfer error associated with the current subtractor circuit and ε_v is the voltage transfer error of the buffered voltage amplifier. Let us assume that g_m and g_π denote respectively the transconductance and the small-signal base conductance of the i-th transistor (i = 1, 2,..., 17), the current transfer error ε_i can be derived as

$$\varepsilon_i \cong \left\{\frac{(g_{mp} + 2g_{\pi p})\left[g_{mn} + g_{\pi n}\left(1 + \frac{2g_{\pi n}}{g_{mn}}\right)\right] - g_{mp}\,g_{mn}}{g_{mp}\,g_{mn}}\right\} \tag{11}$$

where $g_{mn} = g_{m1} = g_{m2} = \ldots = g_{m11} = g_{m14} = g_{m16}$, $g_{\pi n} = g_{\pi 1} = g_{\pi 2} = \ldots = g_{\pi 11} = g_{\pi 14} = g_{\pi 16}$, $g_{mp} = g_{m12} = g_{m13} = g_{m15} = g_{m17}$ and $g_{\pi p} = g_{\pi 12} = g_{\pi 13} = g_{\pi 15} = g_{\pi 17}$. For example, if 0.7μm BiCMOS process parameters are employed under the bias current I_B of 100 μA, then we will obtain ; $g_{mn} = 2.23\times10^{-3}$ A/V , $g_{mp} = 2.14\times10^{-3}$ A/V , $g_{\pi n} = 4.17\times10^{-5}$ A/V and $g_{\pi p} = 4.38\times10^{-5}$ A/V. As a result, the transfer error ε_i of about 6.12 % is expected.

The second error ε_v that is due to the buffered voltage amplifier formed by complementary transistors Q_{14} to Q_{17} can be given by

$$\varepsilon_v \cong \left[\frac{G_w(g_{mn} + g_{\pi n} + g_{\pi p})}{(g_{mn} + g_{\pi n})(g_{mp} + g_{\pi p})} \right] \tag{12}$$

where $G_w = 1/R_w$. With the same process parameters, the resulting voltage gain error ε_v for a load resistance R_w of 10 kΩ is approximately equal to 4.65 %.

For the high frequency responses, the high frequency limitation is strongly depended on the stray capacitances and the current transfer function can approximately be expressed in the relationship of the currents i_z and $(i_p - i_n)$ by

$$\frac{i_z}{(i_p - i_n)} \cong \frac{\left[\frac{g_{mp}}{g_{mp} + 2g_{\pi p}} \right] \left[\frac{g_{mn}}{g_{mn} + g_{\pi n}\left(1 + \frac{2g_{\pi n}}{g_{mn}}\right)} \right]}{\left[1 + \left(\frac{2C_{\pi p} + C_{\mu p}}{g_{mp} + 2g_{\pi p}}\right)s\right] \left\{ 1 + \left[\frac{\left(2C_{\pi n} + C_{\mu n}\right)\left(\frac{g_{\pi n}}{g_{mn}}\right) + \left(C_{\pi n} + 2C_{\mu n}\right)\left(1 + \frac{2g_{\pi n}}{g_{mn}}\right)}{(g_{mn} + g_{\pi n})} \right] s + \left[\frac{(2C_{\pi n} + C_{\mu n})(C_{\pi n} + 2C_{\mu n})}{g_{mn}(g_{mn} + 2g_{\pi n})} \right] s^2 \right\}} \tag{13}$$

where $C_{\pi n} = C_{\pi 1} = C_{\pi 2} = \ldots = C_{\pi 11} = C_{\pi 14} = C_{\pi 16}$, $C_{\mu n} = C_{\mu 1} = C_{\mu 2} = \ldots = C_{\mu 11} = C_{\mu 14} = C_{\mu 16}$, $C_{\pi p} = C_{\pi 12} = C_{\pi 13} = C_{\pi 15} = C_{\pi 17}$, $C_{\mu p} = C_{\mu 12} = C_{\mu 13} = C_{\mu 15} = C_{\mu 17}$ and $C_{\pi i}$, $C_{\mu i}$ denote the emitter-base capacitance and the collector-base capacitance of the i-th transistor, respectively. The denominator of equation (13) has three poles and can be written as

$$D_1(s) = \left(1 - \frac{s}{p_1}\right)\left[1 - s\left(\frac{1}{p_2} + \frac{1}{p_3}\right) + \frac{s^2}{p_2 p_3}\right] \tag{14}$$

where p_i is a pole of equation (13). Usually, the poles p_2 and p_3 are widely separated. If we assume that p_3 is much larger than p_2, the term $1/p_3$ can be neglected compared with the term $1/p_2$ in the denominator. Thus, equation (14) becomes approximately

$$D_1(s) \cong \left(1 - \frac{s}{p_1}\right)\left[1 - \frac{s}{p_2} + \frac{s^2}{p_2 p_3}\right] \tag{15}$$

By equating the coefficients in equation (13) with those in equation (15), the pole positions can be obtained as follows

$$p_1 = -\left[\frac{g_{mp} + 2g_{\pi p}}{2C_{\pi p} + C_{\mu p}}\right] \tag{16}$$

$$p_2 = -\left[\frac{g_{mn} + g_{\pi n}}{\left(2C_{\pi n} + C_{\mu n}\right)\left(\frac{g_{\pi n}}{g_{mn}}\right) + \left(C_{\pi n} + 2C_{\mu n}\right)\left(1 + \frac{2g_{\pi n}}{g_{mn}}\right)}\right] \tag{17}$$

and

$$p_3 = -\left[\frac{g_{\pi n}(2C_{\pi n} + C_{\mu n}) + (g_{mn} + 2g_{\pi n})(C_{\pi n} + 2C_{\mu n})}{(2C_{\pi n} + C_{\mu n})(C_{\pi n} + 2C_{\mu n})}\right] \tag{18}$$

At the port w, the approximate small-signal voltage gain can be written in the term of vw and vz as

$$\frac{v_w}{v_z} \cong \frac{\left[\frac{(g_{mn} + g_{\pi n})(g_{mp} + g_{\pi p})}{(G_w + g_{mp} + g_{\pi p})(g_{mn} + g_{\pi n}) + G_w g_{\pi p}}\right]\left[1 + \frac{C_{\pi n}}{(g_{mn} + g_{\pi n})}s\right]\left[1 + \frac{C_{\pi p}}{(g_{mp} + g_{\pi p})}s\right]}{\left\{1 + \left[\frac{(G_w + g_{mp} + g_{\pi p})C_{\pi n} + (G_w + g_{mn} + g_{\pi n})C_{\pi p}}{(G_w + g_{mp} + g_{\pi p})(g_{mn} + g_{\pi n}) + G_w g_{\pi p}}\right]s + \left[\frac{C_{\pi n}C_{\pi p}}{(G_w + g_{mp} + g_{\pi p})(g_{mn} + g_{\pi n}) + G_w g_{\pi p}}\right]s^2\right\}} \tag{19}$$

The denominator of equation (19) can be rewritten as

$$D_2(s) = \left[1 - s\left(\frac{1}{p_4} + \frac{1}{p_5}\right) + \frac{s^2}{p_4 p_5}\right] \cong \left[1 - \frac{s}{p_4} + \frac{s^2}{p_4 p_5}\right] \tag{20}$$

where we assumed $p_4 << p_5$. The poles p_4 and p_5 can now be estimated by comparing coefficients in equations (19) and (20). Thus we can identify

$$p_4 = -\left[\frac{(G_w + g_{mp} + g_{\pi p})(g_{mn} + g_{\pi n}) + G_w g_{\pi p}}{(G_w + g_{mp} + g_{\pi p})C_{\pi n} + (G_w + g_{mn} + g_{\pi n})C_{\pi p}}\right] \tag{21}$$

and

$$p_5 = -\left[\frac{(G_w + g_{mn} + g_{\pi n})}{C_{\pi n}} + \frac{(G_w + g_{mp} + g_{\pi p})}{C_{\pi p}}\right] \tag{22}$$

In order to figure the high frequency limitation, let us assume that $C_{\pi n} = 8.25\times10^{-14}$ F , $C_{\pi p} = 8.98\times10^{-14}$ F , $C_{\mu n} = 4.14\times10^{-14}$ F and $C_{\mu p} = 4.22\times10^{-14}$ F. Since the poles p_3 and p_5 are the non-dominant poles, the effects of these non-dominant poles are neglected in the calculation. Thus, the poles p_1, p_2 and p_4 are approximately located at 1.5 GHz, 2.67 GHz and 2.14 GHz, respectively. Clearly, the high frequency limitation of the circuit is due to the dominant pole p_1 that is dominated by the transconductance and capacitance associated with the current mirror Q_{12}-Q_{13}. However, this dominant pole p_1 is quite high. Therefore, the circuit can be used in high frequency applications.

Application to Current-Mode Ladder Filters

An approach to derive CDBA-based current-mode ladder filters from passive RLC ladder prototypes will be presented in this section. Due to the low sensitivity nature of doubly terminated RLC ladder filters [R. Schaumann and M.E. Valkenburg. 2001.and P. Huelsman Lawrence. 2000.], this configuration has been receiving a considerable attention. These active implementations are conventionally designed based on the representation of signals as voltages. But in the current-mode based implementation, the input, intermediate and output signals are usually represented as electrical currents that seems to be recognized to offer potential advantage for low-voltage applications. To illustrate the design procedure of CDBA-based current-mode ladder filters by the leapfrog, consider a popular ladder structure that realizes the doubly terminated RLC ladder filter shown in Fig.7. This structure can be characterized by the following expressions

$$
\begin{aligned}
I_1 &= I_S - \frac{V_1}{R_S} - I_2 \quad , \quad V_1 = I_1 Z_1 \\
V_2 &= V_1 - V_3 \quad , \quad I_2 = V_2 Y_2 \\
I_3 &= I_2 - I_4 \quad , \quad V_3 = I_3 Z_3 \\
&\text{M} \\
V_n &= V_{n-1} - V_{n+1} \quad , \quad I_n = V_n Y_n \\
\text{and} \quad I_n &= I_{n-1} - I_{n+1} \quad , \quad V_n = I_n Z_n
\end{aligned}
\tag{23}
$$

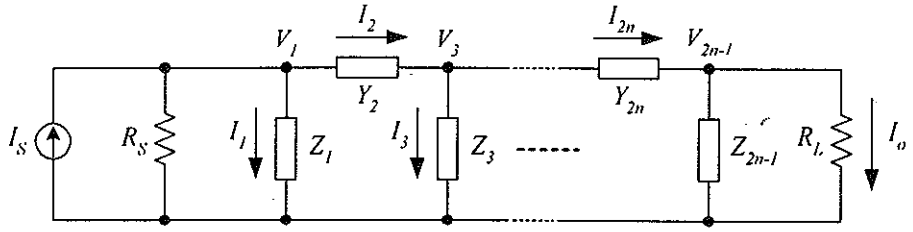


Figure 7 *A general doubly terminated LC ladder network*

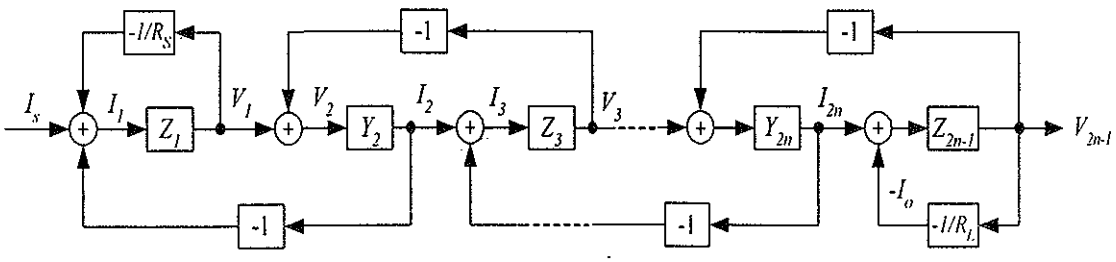


Figure 8 *Block diagram representation of the leapfrog structure*

Using above expressions, a LC ladder filter structure can be represented by the block diagram of the leapfrog realization as shown in Fig.8. Observe that in this figure the repeated use of two operations of Fig.9(a) and 9(c) makes up the complete circuit. These operations can easily be realized by the CDBAs as shown in Figs.9(b) and 9(d). For the CDBA-based filter realization, we can readily obtain the CDBA-RC circuit by interconnecting the corresponding sub-circuits of Figs.9(b) and 9(d) according to the overall block diagram representation of Fig.8. As an example of this design procedure, a current-mode fifth-order Butterworth RLC ladder lowpass filter shown in Fig.10 is realized. The resulting CDBA-based circuit of the filter is shown in Fig.11, where the normalized cutoff frequency ω-3dB = 1 rad/s and the values of resistors and capacitors are in Ω and F, respectively. It can be seen that five CDBAs are employed for implementation of the fifth-order filter. In general, nth CDBAs are required for realizing the nth-order filters. On the other hand, CCII-based implementation in voltage-mode designs of this structure requires some additional devices when they are used for cascading sections due to the high-output impedance [E.I. El-Masry. 1996. and S.I. Liu. 1991.]. It should be noted that the CDBA-based ladder leapfrog filter implementations can reduce the number of active components by approximately 50% comparing with CCII-based [E.I. El-Masry. 1996. and S.I. Liu. 1991.] and OTA-based [J. Wu and E.I. El-Masry. 1998. . Deliyannis. Y. Sun and J.K. Fidler. 1999 and J. Wu. and E.I. El-Masry. 1998.] filter implementations, and less than 50% when comparing with the realizations using Op-Amps [R. Schaumann and M.E. Valkenburg. 2001. and P. Huelsman Lawrence. 2000.]

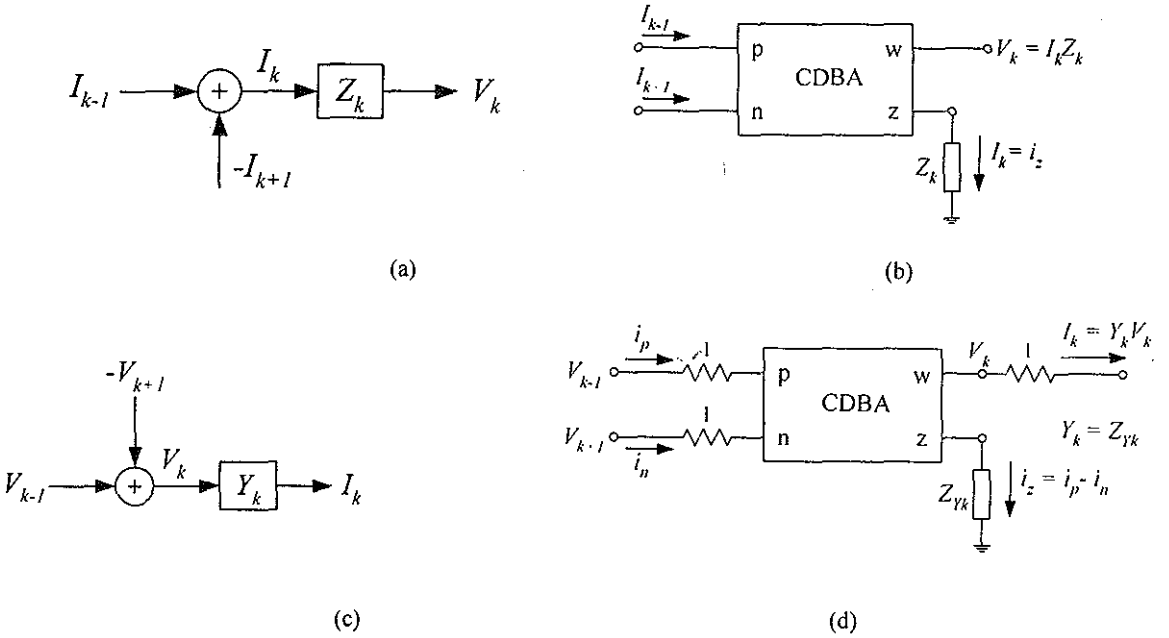


Figure 9 *Sub-circuits and their realizing operation using CDBAs*

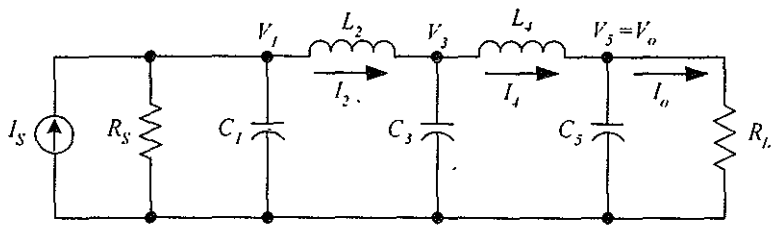


Figure 10 *Current-mode fifth-order Butterworth RLC ladder lowpass filter*

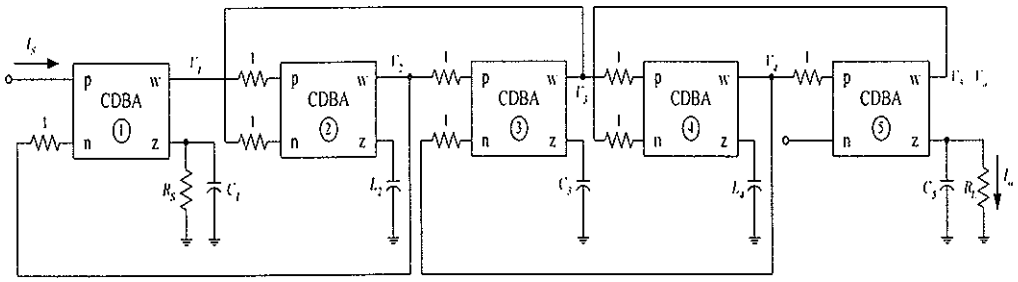


Figure 11 *CDBA-based realization of the current-mode fifth-order lowpass filter of Fig.10*

This technique can also be used to design RLC bandpass filters. A sixth-order RLC bandpass filter is shown in Fig.12, which includes parallel and series resonant circuits as sub-circuits. The sub-circuits of the filter are realized by using CDBAs as shown in Fig.13. Thus the whole structure can be shown in Fig.14.

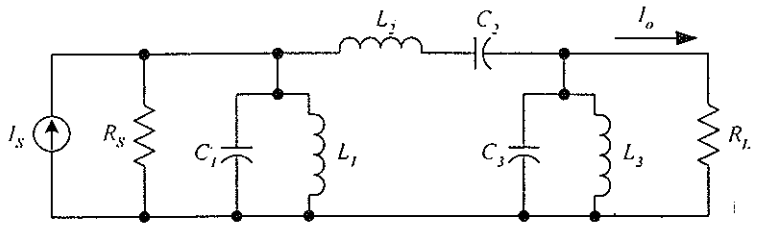
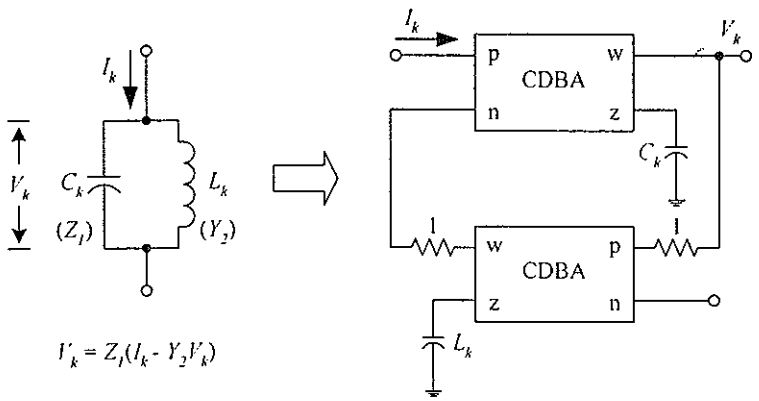
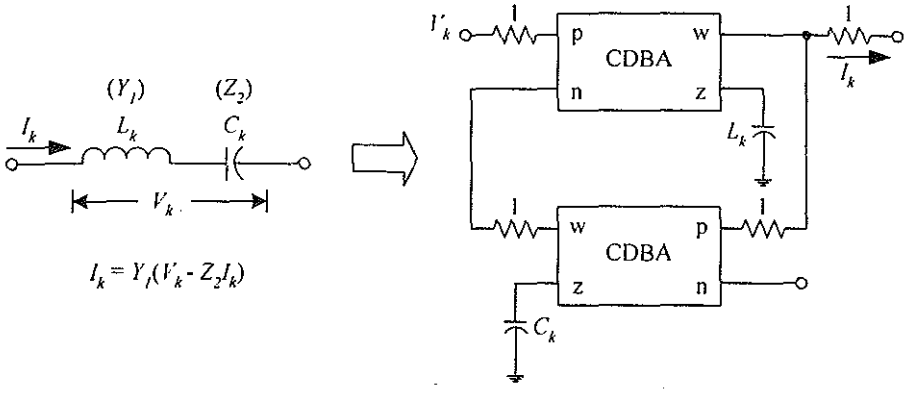


Figure 11 *Current-mode sixth-order RLC ladder bandpass filter*



(a)



(b)

Figure 13 *Sub-circuits of the filter of Fig.12 involving CDBAs*

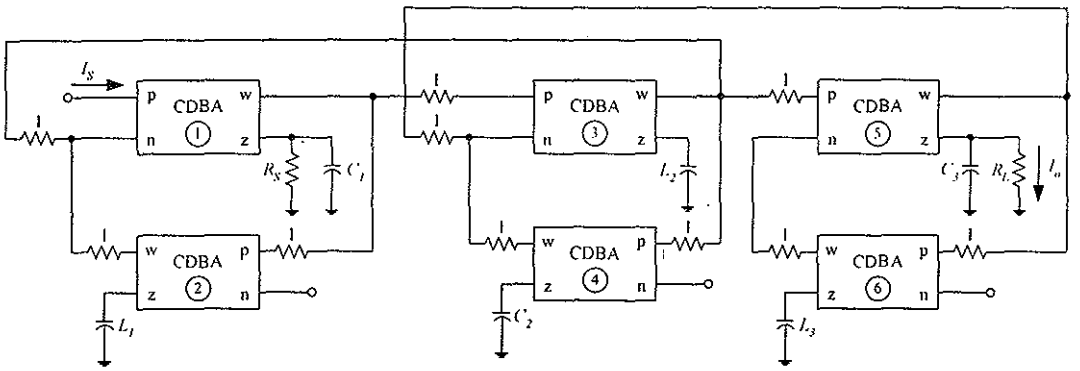


Figure 14 *The current-mode sixth-order bandpass filter using CDBAs*

Design Examples and Simulation Results

The performances of the proposed low-voltage CDBA of Fig. 6 were confirmed using PSPICE simulation with the 0.7μm BiCMOS process parameters. The power supply voltage is ±V = ±1 volts and the bias current I_B is 100 μA. The simulated DC offset current at the port z, for R_z = 1 kΩ, is very low and is approximately equal to 3.23 μA, and the simulated DC voltage transfer characteristic between the voltages v_z and v_w, for R_w = 10 kΩ, has the DC offset voltage value of about 1.98 mV. The total power consumption was found by the simulation to have a low value of 1.84 mW. Fig.15 shows the simulated frequency responses of the current and voltage transfer characteristics of the proposed CDBA. It is clearly seen from the figures that the bandwidth frequencies in the range of hundred MHz are obtained. The simulation results show that the circuit has a wide bandwidth and low-power consumption.

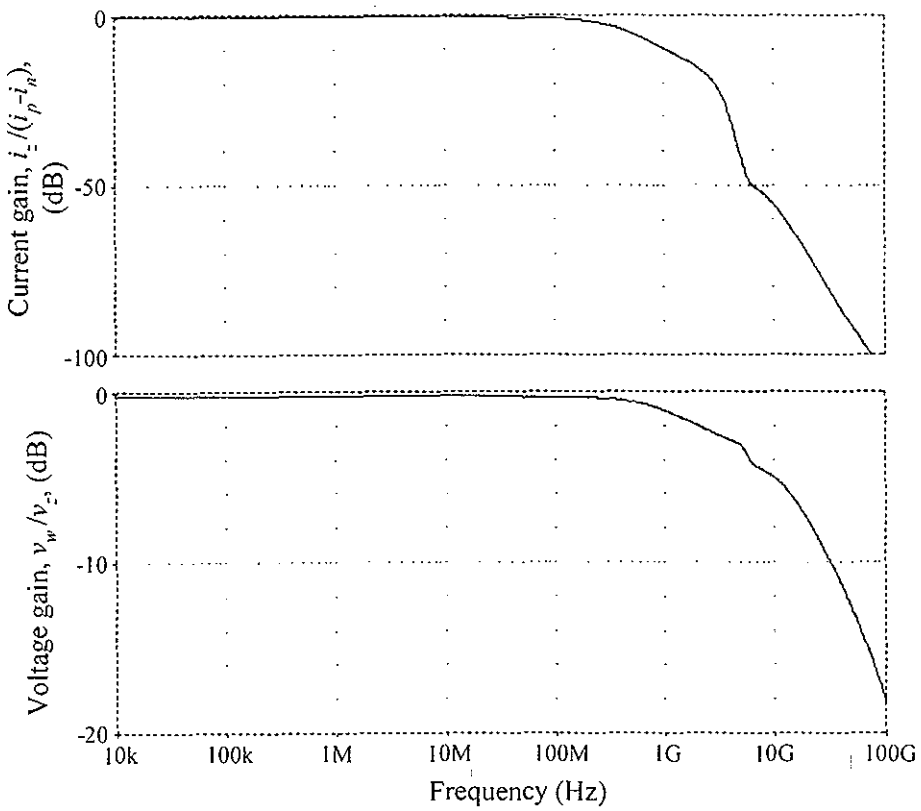


Figure 15 *Simulated frequency responses of the proposed CDBA*

As an illustration of a current-mode fifth-order Butterworth lowpass filter, the filter of Fig.10 with a –3dB frequency ω_{-3dB} of 100 Mrad/s was designed. This condition leads to the passive element values as follows ; $R_S = R_L = R = 1$ kΩ, $C_1 = C_5 = 6.18$ pF, $L_2 = L_4 = 16.18$ pF, and $C_3 = 20$ pF. The simulated and theoretical responses are shown in Fig.16.

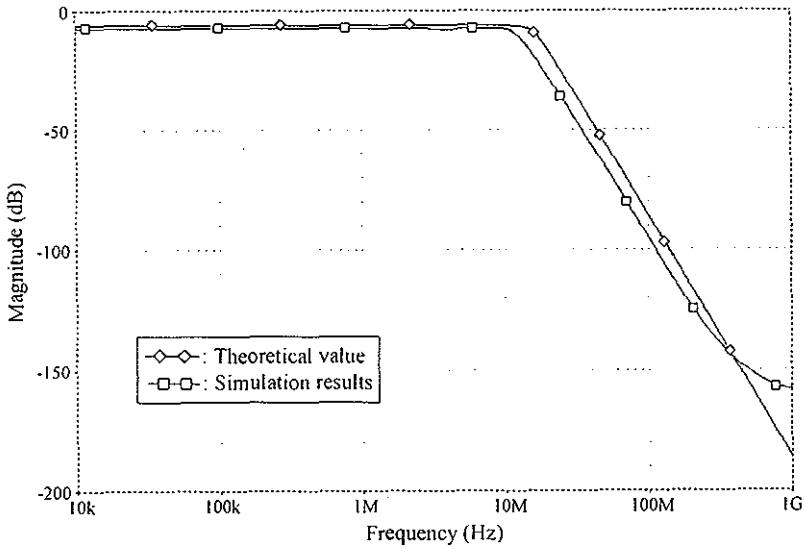


Figure 16 *Simulated responses for the fifth-order Butterworth lowpass filter of Fig. 11*

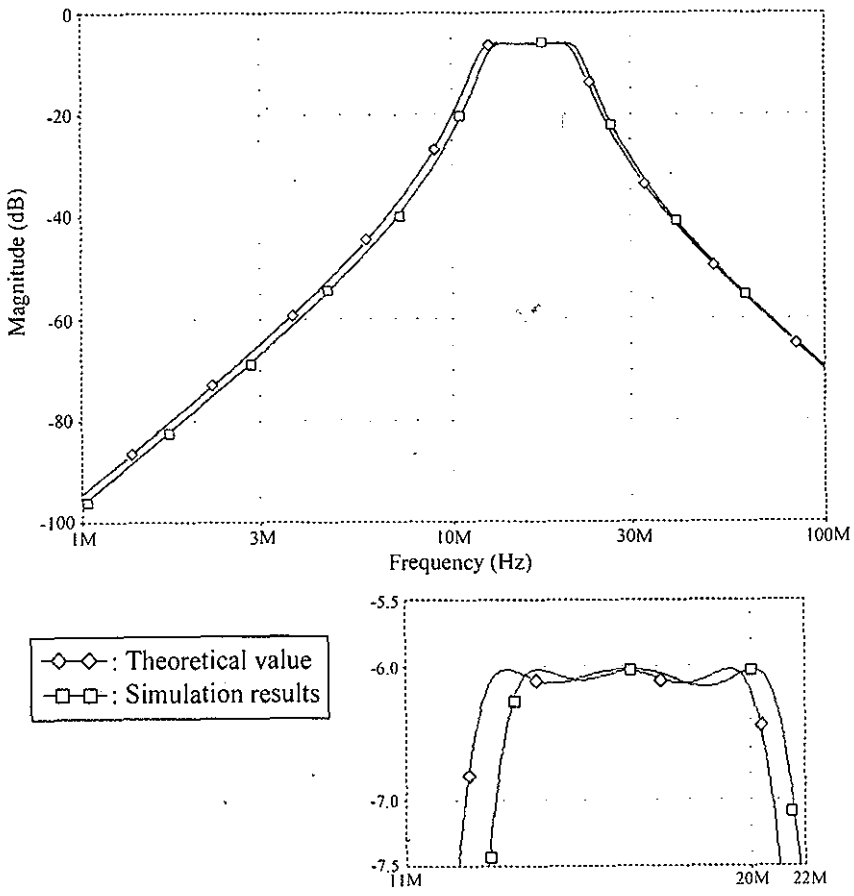


Figure 17 *Simulated responses for the sixth-order Chebyshev bandpass filter of Fig. 14*

For illustrative purposes, a sixth-order Chebyshev bandpass filter was also designed with the following specifications ; ω_{3dB} = 100 Mrad/s, bandwidth (BW) = 0.45, and passband ripple = 0.1 dB. These specifications resulted in the following components values ; $R_S = R_L = R$ = 1 kΩ, $C_1 = C_3$ = 22.923 pF, C_2 = 3.921 pF, $L_1 = L_3$ = 4.362 pF, and L_2 = 25.498 pF. The simulated responses of the designed filter together with the theoretical values are shown in Fig.17.

Conclusions

A design technique for realizing the low-voltage current differencing buffered amplifier (CDBA) and its application to implement continuous-time current-mode leapfrog ladder filters has been described. The proposed circuit can operate at a low power supply voltage as well as high-frequency operations, and can easily be implemented in a monolithic integrated circuit. The simulated responses with PSPICE are quite good over a wide frequency range and the circuit requires low-power consumption. As seen from applications, we prove that it is very suitable for realizing any current-mode leapfrog ladder filters employing CDBAs as an active element. The proposed technique requires n^{th}-CDBAs for the realization n^{th}-order ladder filter, which is a significant active element reduction in comparison with the previously reported methods using Op-Amps, OTAs, and CCIIs.

Acknowledgment

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