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Low power area efficient self-gated flip flop: Design, implementation and analysis in emerging devices

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Abstract

This study presents a novel CMOS self-gated flip flop for low power and area efficient applications. The low power operations are achieved by deactivating the clock signal when not required in the circuit. The study explores the proposed design in emerging devices like Carbon Nanotube Field Effect Transistor (CNTFET), Graphene Nano-Ribbon FET (GNRFET) and FinFET devices. The simulations are carried out at 16nm technology node in HSPICE with nominal conditions of 0.9 V supply voltage, 25% data activity at temperature of 25 °C and frequency of 400 MHz. Results obtained shows that the proposed design consumed the least power with a reduction of minimum 53.68% and maximum 81.39% at variations in voltages ranging from 0.9 V to 1.2 V. The overall power delay product (PDP) at nominal conditions is reduced by minimum 61.45% and maximum 80.81%. The proposed flip flop is also an area efficient design having least number of transistors and minimum sum of width with average reduced area of 29.55%. The proposed design, when implemented and simulated with emerging devices, showed significant improvements in power consumptions and speed of operations. The simulations confirmed that the FinFET counterpart of the proposed design is most power efficient device whereas GNRFET the least. But the GNRFET is the fastest of all the devices followed by CNTFET at second and FinFET as third fastest whereas CMOS is the slowest among all these devices.

Keywords: Self-gated, CMOS Digital circuit, CNTFET, GNRFET, FinFET

1. Introduction

In central processing unit (CPU) based semiconductor circuits, flip flops (FFs) are the most often used standard cell. The number of flip flops within a specific CPU design increases as the number of CPU core increases in tandem with the progress of CPU technology. The input data fed to flip flops has very less changing activity during normal operations of CPU, however, the internal clock continues to toggle and consume power. In comparison to all other conventional cells used in CPU-based semiconductor circuits, flip flop demands the most power. Even when the input data to the flip flop has low change activity, the internal clock power usage continues to consume power at every clock cycle [1]. The high power consumption reduces the battery life of mobile devices, increases heat within devices, which leads to performance degradations and raises the overall cost of maintaining and operating stationary devices such as computer servers or desktop systems.

In a synchronous architecture, all the flip flops receive the clock signal at the same time. However, non-idealities of the clock distribution are frequently caused by the parasitic effects generated during the distribution of the clock signals, and to varying degrees by interconnect across the chip, as well as limits arising from a variety of reasons. They can produce apparent jitter and clock skew by causing temporal and spatial fluctuations in the clock signal [2]. The synchronous circuits, must, nevertheless, contribute to as little delay as probable while consuming as little power as possible. As a result, it's critical to concentrate on the clock synchronization circuit's power economy and signal integrity [3]. It is necessary to limit the power dissipation of flip flops in circuits with a large number of clock endpoints. Low power consumption in turn helps to increase the device reliability [4]

The clock distribution network consumes up to 70% of power in low power applications and is a significant contributor to total power in advanced microprocessors [5]. Additionally, the challenging performance and growing complexity in high-speed very large-scale integration (VLSI) systems increases the clock power. A clock system is used to govern the system timing parameters. A clock system is an essential component of every synchronous system. Even in a well-designed system, several factors such as radiation environment, different voltage supplies, temperatures and parasitics in the connecting channels might cause a delay variation between two identical clock lines [6]. The clock edge inaccuracy, also known as clock skew, is the discrepancy between the actual and projected arrival times of this clock edge. It's the sum of all pathways' worst-case timing inaccuracies. The majority of the designs cannot withstand a skew of more than 10% of the time span. The system function is harmed if the system clock skew exceeds the design limits [7].

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The need to develop low-power designs in order to allow the increase in chip functionality is the demand of the industry. Several such approaches have been proposed [8-19]. Gating has demonstrated to be successful and a sensible reduction in power consumption and can be accomplished specifically for circuits with low input signal switching activity [20]. In such circumstances, each flip flop has its own gating logic, and the overhead introduced must be kept to a minimum. Self-gated clocking approach has evolved as a viable option for low-power clocking.

The paper presents a novel low power and area efficient self-gated flip flop and explores the design beyond CMOS. Section 2 presents the review of existing recent state of art self-gated flip flops. In section 3 the proposed novel self-gated flip flop is discussed. Section 4 presents the simulation power, PDP, area results and tests for the proposed design at more complex circuitries. Section 5 explores the novel design in emerging devices with a quantitative and extensive comparison in CMOS, beyond CMOS and with existing designs.

2. Self-gated flip flops

The most widely used flip flop on a semiconductor chip in a digital circuit is the master slave flip flop which may receive a gated input clock signal from a slave latch. This gated clock signal is dependent on a non-gated clock signal and may also be dependent on a clock gating condition. Self-gated as the name says will generate this condition known as a control signal within the circuit. As in D flip flop the output has to follow the input, the non-gated clock which is switching continuously and dissipating power may be controlled using a gated mechanism. The mechanism disables the clock when not needed i.e. at the time when output and input doesn't change, hence savings all the unnecessary internal switching. At the time when output and input differ, the clock gets enabled. This control mechanism is generated within the flip flop and without any external signal. One such design was proposed by Nafziger in [21] as shown in Figure 1. This flip flop circuit uses a simplified conditional technique for reducing power consumption. The control signal here is an OR-AND-INVERTER (OAI) circuit. One input to the AND-INVERT is the non-gated clock signal (CLK) and the other is the output of the inverted value of master latch transmission gate (TG1) and output (A and QF). A conditional gated clock signal (CLKP) is generated using this OAI circuit which is fed to the slave transmission gate (TG2). When the flip flop state and the data input have the same logic (logic 0), the slave latch's conditional clock inputs maintain the slave transmission gate opaque. A change in the non-gated clock turns the slave TG2 ON. The fact that a flip flop's state does not change frequently and that the majority of flip flops store a low logic value may be exploited by an OAI circuit. There is no need to supply a clock signal to the slave latch if the flip flop will not change state or have the same logic prior to the arrival of the received clock signal.

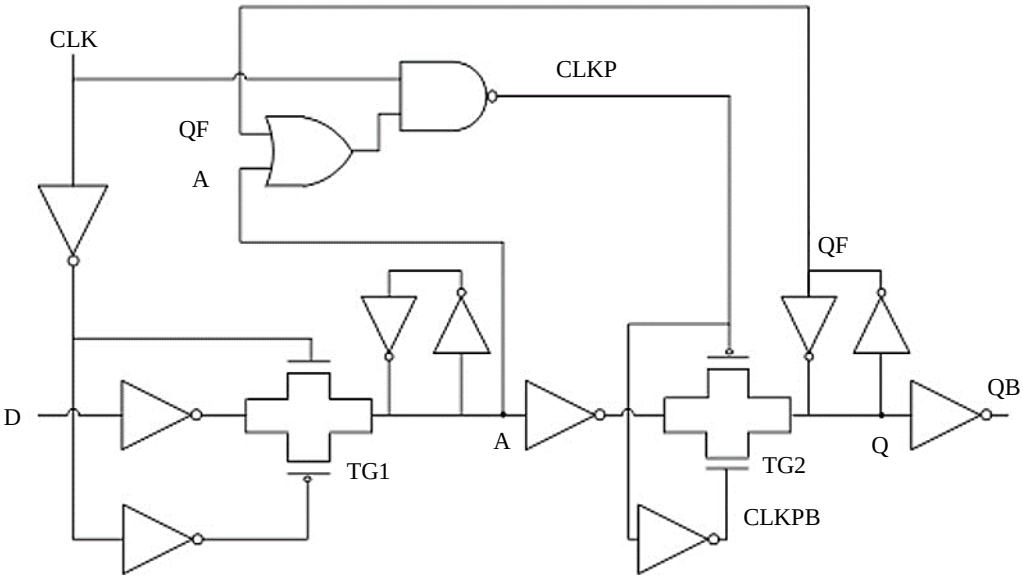


Figure 1 Architecture of Nafziger's FF [21]

Figure 2 proposed by [22] is another example of self-gated flip flop. This circuit contains a latch that is set to update its stored state in accordance to a pulsed clock signal and input data signal. A pulse generator is used in the circuit to generate the controlled clock signal (CLKP) from an input data signal (D), non-gated clock signal (CLK), a latch feedback signal (QF) and latch output (Q). In the pulsed clock signal, the method involves changing a latch's stored state to correspond to the state of an input data signal. The technique entails activating the pulse in response to a clock signal with a first level and the stored state corresponding to a first logic level of a previous input data signal that differs from a second logic level of the input data signal. The approach comprises deactivating the pulse in response to a second-level clock signal. The pulse clock signal generated has a fixed signal level in accordance to the previous input signal with same logic levels. The circuit used to generate the clock pulse (CLKP) signal here is a comparator which compares the input data signal with the feedback output. The output of the comparator generates a signal which indicates whether a change in input data and output has taken place or not.

Rasouli in [23] proposed a semi self-gated flip flop as shown in Figure 3. When the clock signal is one (i.e. CLK=1), signal CLKB will be zero, the slave latch AND gate outputs a zero to the slave latch NOR gate's one input. As a result, the latch NOR gate acts as an inverter, inverting the output of the master latch circuit. The slave latch inverter generates the required output Q. When the CLK=0, CLKB will be high causing the slave latch NOR gate to function like an inverter complementing the output of the slave latch AND gate. Thus the slave latch NOR gate is ideally coupled with inverter generating output QF. The pulse signal generated at P2 is not small pulses at input data transitions rather a controlled input clock train which enables clock signal only at input high values and disables at low input. Thus the flip flop is not completely a self-gated flip flop but instead is a semi gated flip flop.

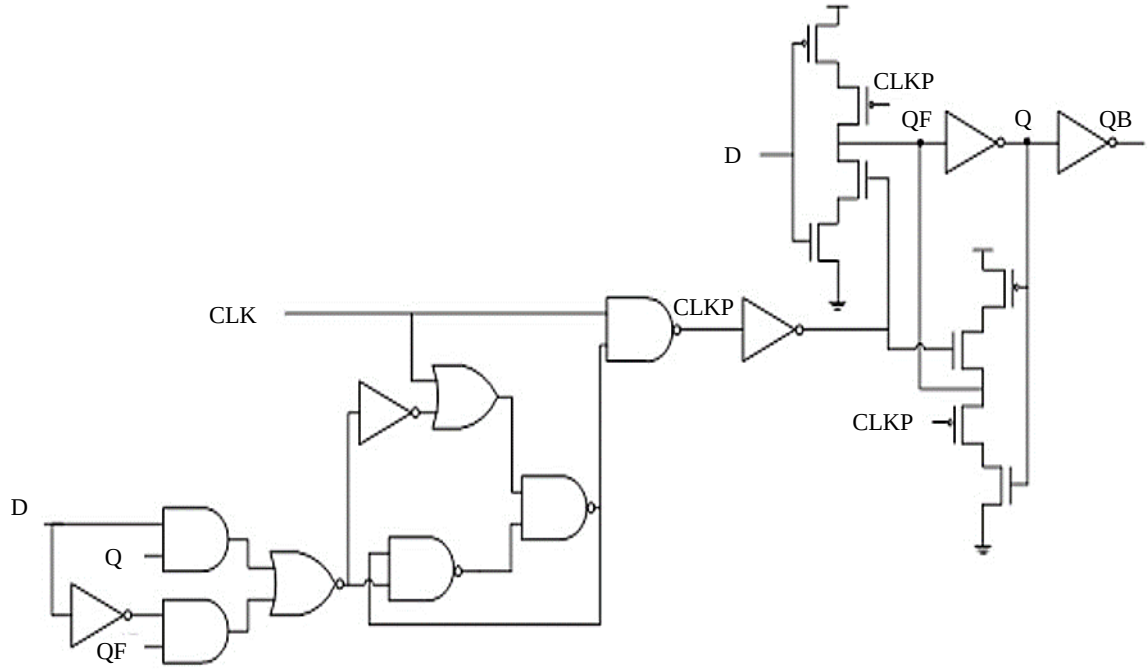


Figure 2 Architecture of Vickers FF [22]

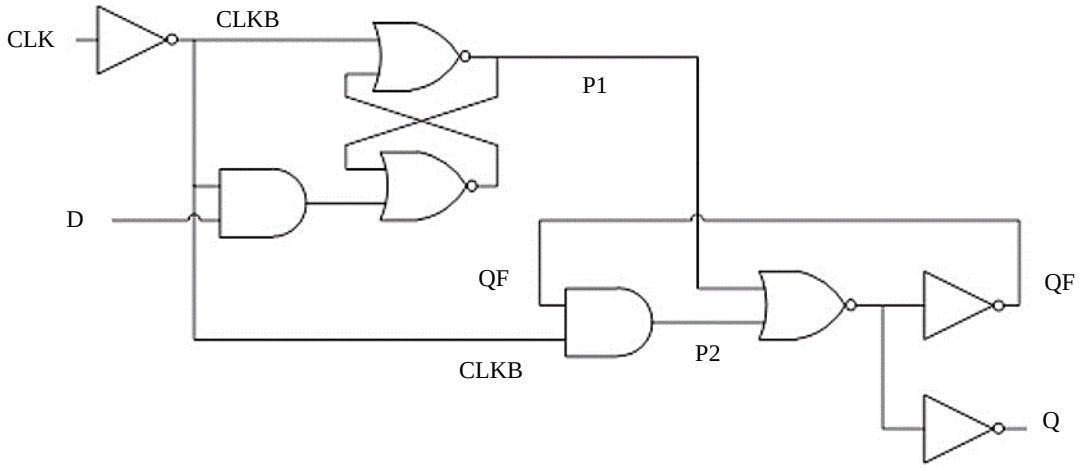


Figure 3 Architecture of Rasouli's FF [23]

3. Proposed self-gated flip flop

The proposed CMOS based self-gated flip flop is shown in Figure 4. The design basically is a master slave flip flop with a comparator output as the control signal. The comparator compares the input signal 'D' and the output signal 'Q' and generates an output which controls the internal clock signal to the master slave flip flop. The use of comparator eliminates the unnecessary switching of the input non-gated clock signal and their by saving power.

In the proposed flip flop, the non-gated clock is fed as the input of the transmission gate TG1 which is controlled by the output of the comparator signal 'G' and its complement 'GB'. The output generated by TG1 is the conditional clock (CLKP) used as clock inputs to the master slave flip flop. This output is only the pulses which are generated at the changes in the input and output signals 'D' and 'Q'. The pulse will be generated at every high to low and low to high transition of input data signal 'D'. The width of this pulse is dependent upon the input clock transition from high to low. The master latch constitutes of one transmission gate (TG2) and one inverter (INV3) connected back to back and the output of which is fed to the slave latch which comprises of one transmission gate (TG3) and two inverters (INV4 & INV5). The second inverter here (INV5) in the slave latch is a weak feedback inverter used to drive the output 'Q'. The comparator circuit is made of two nMOS (N1, N2) and two pMOS (P1, P2) devices.

When the gated clock signal (CLKP) is high, the master latch will pass the input 'D' to the intermediate node 'I' whereas the slave latch during this period is disabled. When the gated clock signal is low, the master latch is disabled and holds the value at the intermediate node 'I' and the slave latch gets enabled. The slave latch now passes the data that is stored at node 'I' to the output 'Q'. The keeper circuit used at the output of the slave latch holds the value at node 'Q' when the gated clock is disabled at slave latch. Therefore master latch will be active when CLKP is high and inactive when CLKP is low whereas slave latch will be active when CLKP is low and inactive when CLKP is high. The same can be seen and is demonstrated in the operational waveforms of the proposed flip flop in Figure 5.

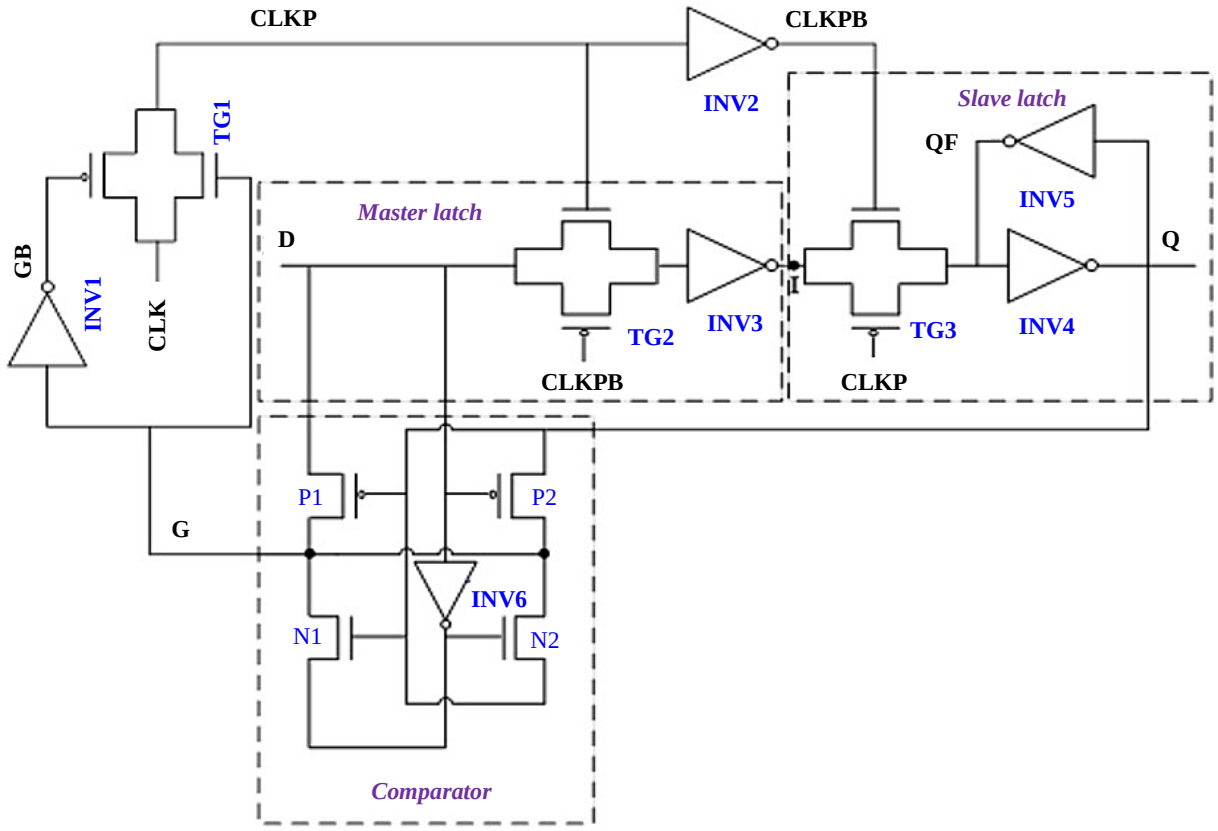


Figure 4 Proposed self-gated FF

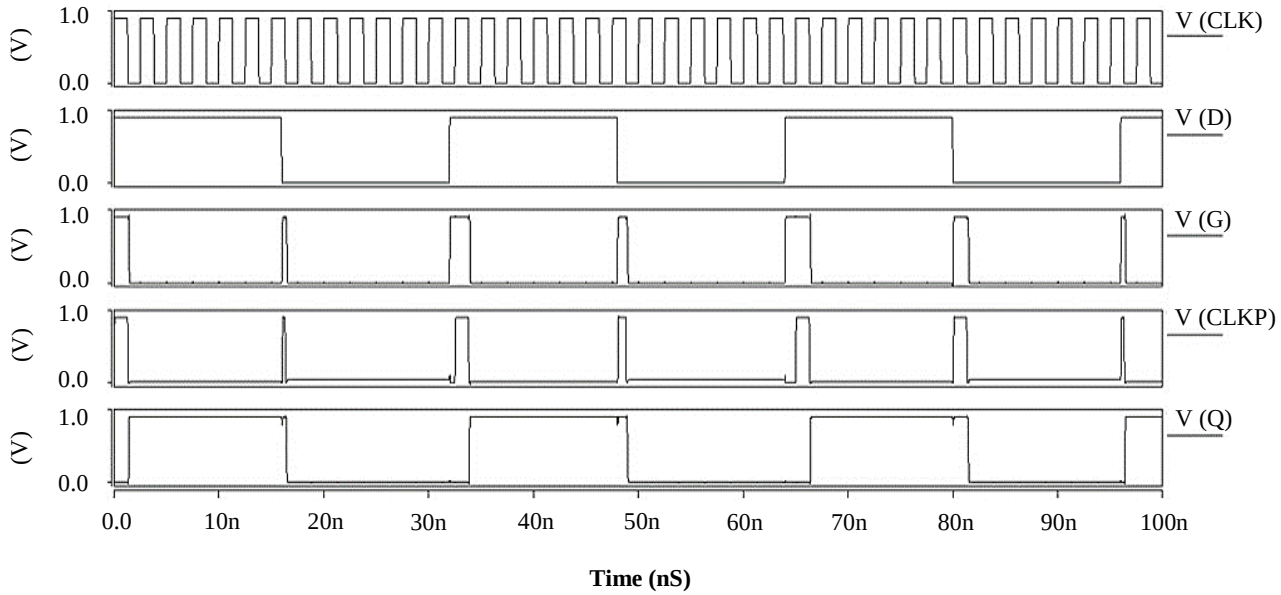


Figure 5 Transient waveforms of proposed self-gated flip flop

4. Simulation results and discussions

The proposed self-gated flip flop and the existing designs reviewed in section 2 are at first simulated in 16 nanometer CMOS technology node using the PTM model in H-SPICE simulator. All design where optimized using size tweaking for the optimal trade-off between power and CLK to Q delay. The nominal conditions are 400 MHz input clock frequency at a temperature of 25 °C with operating voltage of 0.9 V. Since gated flip flops are better suited for low data activity circuits, the nominal data activity taken into consideration in this work is 25% and a 16-bit data length is used. Table 1 shows the average power consumption of flip flops at variation in voltages from 0.9 V to 1.2 V. As evident from this table, the proposed self-gated flip flop consumes the least power at all different voltage levels.

Table 1 Average power (uW) at variations in supply voltage

Supply voltage	0.9 V	1 V	1.1 V	1.2 V
Nafziger's FF	1.38	1.6	1.81	2.26
Vickers FF	0.95	1.18	1.45	1.78
Rasouli's FF	2.06	2.5	3.1	3.87
Proposed FF	0.44	0.51	0.59	0.72

In terms of CLK to Q delay, the proposed flip flop was second fastest but nearly at par with the Nafziger's FF which was the fastest of all. But the overall PDP of the proposed FF as shown in Figure 6 is by far the least among all the compared designs making it a viable option for low power and portable electronics. Besides the power benefits, the other advantage of the proposed design is in its area overhead. The proposed design in terms of number of transistors has only 22 transistors on board which is minimum among all the designs. Figure 7a shows the transistor requirements of all the flip flops. The proposed flip flop has also the least sum of widths (W) of all transistors as shown in Figure 7b. Figure 7a and 7b clearly indicates that the proposed flip flop is area efficient and requires less area when compared to other designs.

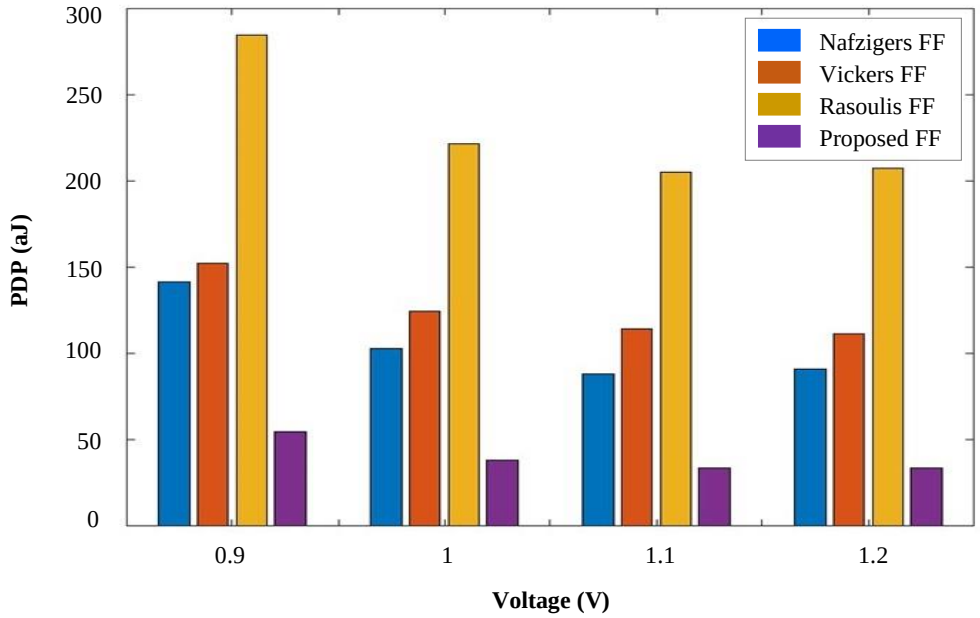


Figure 6 PDP at variations in supply voltage

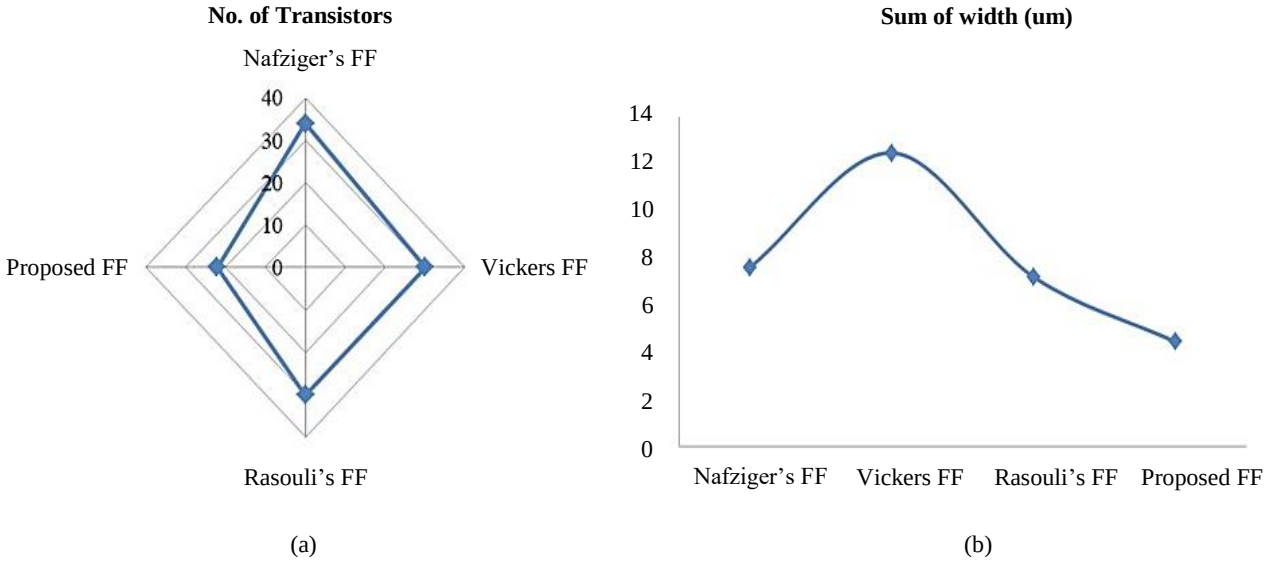
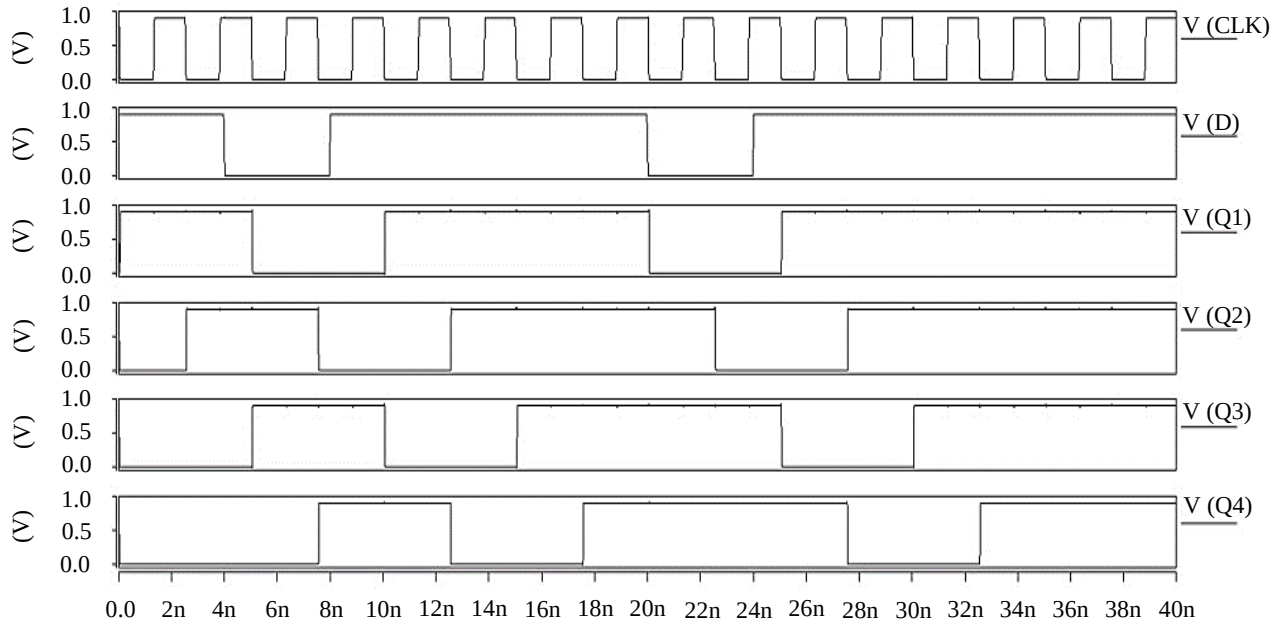
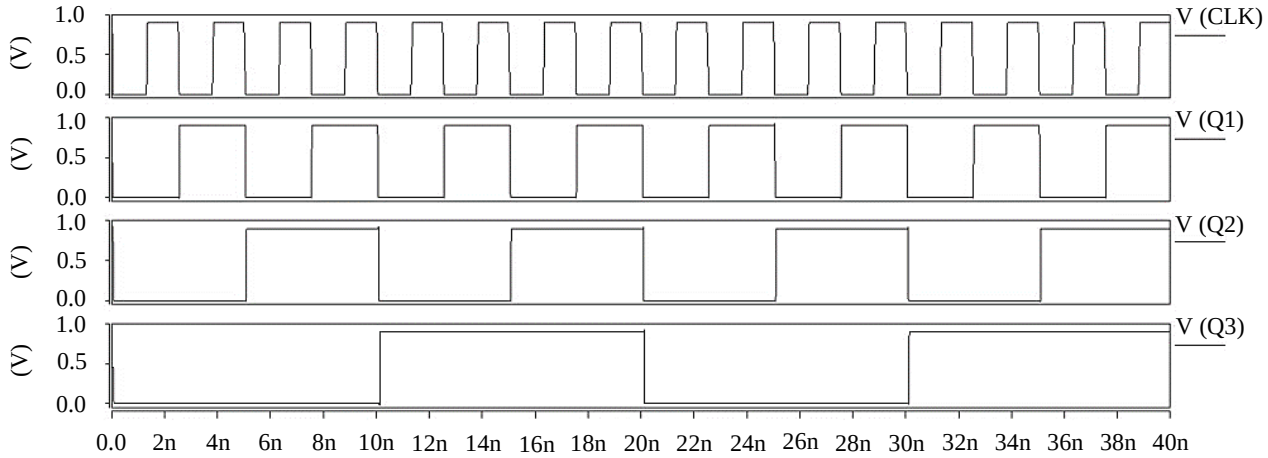


Figure 7 Area requirements (a) transistor count of FFs (b) sum of width of FFs

In order to demonstrate and verify the correct logical functionality of the proposed design, the proposed self-gated flip flop is tested for applications in complex circuitries. This test was performed under the simulation environments of same nominal conditions and the flip flop was tested as a 4-bit shift register and a 3-bit frequency divider. Figure 8 validates and showcases the proposed design's worthiness in digital CMOS devices.



(a)



(b)

Figure 8 Application as (a) 4-bit shift register (b) 3-bit frequency divider

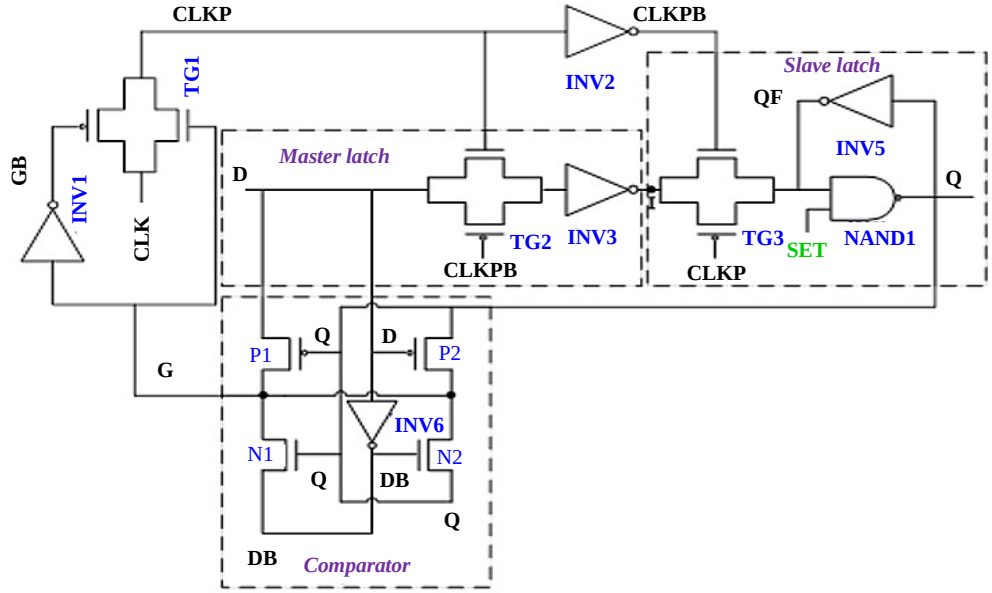
The proposed self-gated flip flop design can also be implemented with asynchronous SET and asynchronous RESET signals. This configuration is shown in Figure 9. Figure 9a represents the proposed circuit with asynchronous SET signal where the invertor INV4 in Figure 5 is replaced with a NAND gate. One input of the NAND gate can control the SET operation whereas the second input is fed from the output of the transmission gate TG3. When the SET signal is low, the output Q will always be high regardless of the input data and the gated clock. When the SET signal is high, the flip flop will function normally as discussed in section 3. Figure 9b shows the proposed circuit with asynchronous RESET signal where a NOR gate instead of NAND is used. When the RESET input is high, the output Q will always be low regardless of the input data and the gated clock. When the RESET input is low, normal operation of the flip flop takes place.

The operation with SET and RESET signals is also shown in Table 2. The proposed flip flop in Figure 9 are further tested for wide frequency range. The frequencies were varied from nominal frequency of 400 MHz to 2 GHz. The proposed flip flop was found functional at all tested frequencies the results of which are shown in Figure 10.

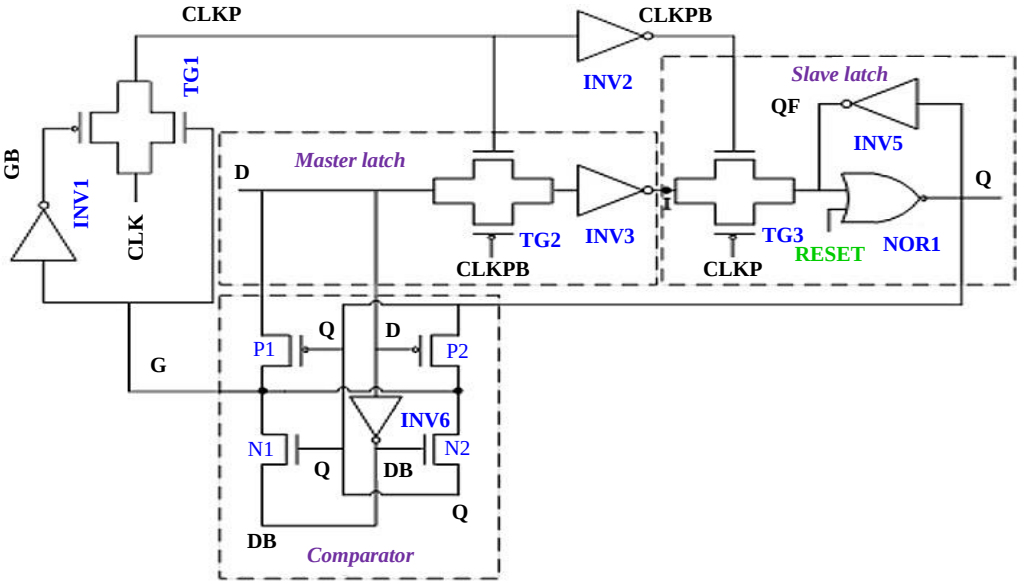
Table 2 Flip flop operation with SET and RESET signals

Signal	Gated clock	Input	Output
SET-0	X	X	1
SET-1	Falling edge	D	D
RESET-1	X	X	0
RESET-0	Falling edge	D	D

X: Logic 1/0



(a)



(b)

Figure 9 Proposed flip flop with (a) Asynchronous SET (b) Asynchronous RESET signals

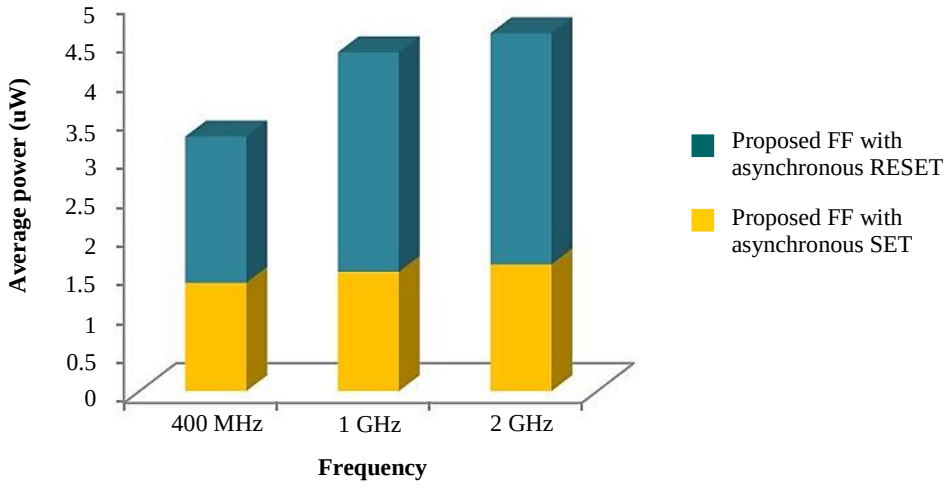


Figure 10 Average power at variations in frequencies

5. Analysis in emerging devices

Scaling of CMOS, although on-going, will come to an end as the short channel effects has become a critical parameter. Researchers have explored new devices beyond CMOS. Apparently same CMOS architecture can be used to analyze beyond CMOS devices. One of the most used emerging devices recently is the CNTFET because of its similar electrical characteristics and structure to MOSFET. Furthermore CNTFETs show reduced sub-threshold swing and gentler short channel effects than CMOS [24]. The CNT is used as a path to escort electrons from source to drain. The parameters of CNTFET like length, type of semiconductor used and gate insulator thickness affects the CNT characteristics [25]. Genetic algorithm for CNTFET proposed by [26] has shown better results and improved efficiency. Another emerging device is the FinFET technology which consists of silicon Fins mounted with independent multiple gates or shortened gates. These Fins are usually on silicon-on-insulator (SoI) substrate. For shortened gates, to turn ON the device, maximum gate drive is provided when the two gates are biased together whereas for independent gates, biasing of the gates is electrically independent [27]. FinFET technology also allows designers to operate circuits at substantially lower supply voltage compared to other technologies and has the advantage of control of the electric field in the channel region [28]. The third type of emerging device in use and in testing recently is the GNRFET. Due to its exceptional physical and electrical characteristics, graphene has drawn considerable interest as a foundation material for nanoelectronic devices. There are two types of GNRFETs, MOSFET-type GNRFET (MOSGNR) and Schottky-barrier type GNRFET (SBGNR) [29]. The reservoirs of MOSGNR are doped with acceptors or donors. Metals are employed as contacts while graphene serves as the base channel material in SBGNR, which causes SBs to develop at the interfaces. SBGNRs have the benefit of not requiring any extra doping in the contacts or the channel. As a result, it lessens the fabrication's technical challenges and removes doping variance. Due to its ambipolar tendency, the SBGNR has a downside that limits performance, and in comparison to MOSGNR, it has a poor I_{ON}/I_{OFF} ratio [30]. Graphene may also be compatible with the current silicon CMOS manufacturing process and ideal for the creation of flexible electronics due to its thin, flat, and strong lattice. Graphene nanoribbons (GNRs) that have been successfully produced have shown widths as small as 10 nm or less, are of good quality, and have relatively smooth output edges [31].

The proposed self-gated flip flop is explored in these three emerging devices along with CMOS technology for performance experiments. The same nominal conditions are kept as in CMOS in previous section, the number of tubes used in CNTFETs are 3, number of Fins in FinFETs are 3 and number of ribbons used in GNRFETs are also 3 for fair comparison. Table 3 shows the power analysis of existing flip flop, proposed flip flop in CMOS, in CNTFET, in GNRFET and in FinFET devices at variation in data activities and at different frequencies. Also calculated is the optimal PDP of all flip flops at nominal operating conditions. The power consumption of proposed self-gated CMOS circuit is minimum at all variations in data activity except at 0% activity (all the data high) where it is nearly at par with Vicker's FF. When emerging devices are taken into account, it is observed that FinFET technology consumes ultra-low power whereas GNRFET cannot be considered for low power designs as the power consumption increases drastically at mere increase in activity. Likewise because of so low power consumptions, the PDP of proposed design in FinFET is least followed by proposed design in CNTFET. Small changes in average power are observed in the proposed designs in FinFET and CMOS when the clock frequency varies, as this should ideally be the case due to the use of gated clock signal. The variation of frequency had a huge impact on GNRFET based device and because of this the GNRFET as of now cannot be considered as a device for low power design.

Table 3 Power analysis of flip flops

Flip flops	Nafziger's FF	Vickers FF	Rasouli's FF	Proposed CMOS	Proposed CNTFET	Proposed GNRFET	Proposed FinFET
Optimal PDP at nominal voltage (aJ)	141.45	152.30	284.20	54.53	20.19	829.97	4.77
Avg. Power at nominal conditions (uW)	1.379	0.940	2.061	0.436	1.417	456.030	0.192
Avg. Power at 12.5% activity (uW)	1.066	0.482	2.317	0.237	3.090	10.660	0.114
Avg. Power at 0% activity-all 1 (uW)	0.616	0.030	3.134	0.039	8.293	4.219	0.024
Avg. Power at 0% activity-all 0 (uW)	1.234	0.269	0.590	0.066	0.114	4.156	0.003
Avg. Power at 200 MHz (uW)	0.903	0.830	1.089	0.402	1.204	8.342	0.192
Avg. Power at 800 MHz (uW)	2.073	0.954	3.856	0.439	2.396	2207	0.195

Table 4 shows the speed of operation of all the flip flops at variation in temperature. It is quite clear from this table that the CMOS devices are the slowest of all. GNRFET which consumes most power is the fastest device with almost negligible delay. CNTFET is the second fastest followed by its FinFET counterpart. At nominal operating conditions, the GNRFET is minimum 98.23% faster than CMOS devices, the CNTFET is minimum 86.13% and FinFET minimum 75.45% faster to CMOS's.

Table 4 Clock to output delay measurements at variations in temperature

Flip flops	Nafziger's FF	Vickers FF	Rasouli's FF	Proposed CMOS	Proposed CNTFET	Proposed GNRFET	Proposed FinFET
CLK-Q delay at 0 °C (pS)	72.11	118.10	102.66	88.51	17.98	1.81	25.85
CLK-Q delay at 25 °C (pS)	102.50	160.32	137.96	123.93	14.22	1.81	25.16
CLK-Q delay at 50 °C (pS)	140.00	208.07	177.04	163.95	15.34	1.81	24.43
CLK-Q delay at 75 °C (pS)	182.25	259.89	219.26	208.34	18.88	2.68	22.40
CLK-Q delay at 100 °C (pS)	223.63	316.86	264.76	253.06	15.60	1.81	20.55

6. Conclusions

A novel power and area efficient self-gated flip flop is proposed and analyzed in CMOS, CNTFET, GNRFET and FinFET devices. FinFET counterpart of the proposed design consumes least power and has minimum PDP which makes it very suitable for robust low power circuits. Among all the devices, GNRFET as of now is not recommended for low power flip flop memory design rather it can be used for high performance circuits requiring extremely fast operations and where power is not a factor of concern. The simulation

result confirms the superiority of FinFET in terms of power efficiency and GNRFET in terms of speed of operations. Furthermore, CMOS and FinFET based logic circuits demonstrated improved power consumption at frequency variations. Not only this, the area advantage of the proposed design in CMOS supersedes the latest available self-gated architectures with a reduced area overhead by minimum of 26.67% and maximum of 35.30%.

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