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A 1.2V, low-power, and high linear UWB down-conversion CMOS mixer

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Abstract

A low voltage, high linearity and gain with low power ultra-wideband (UWB) CMOS mixer in the RF receiver is proposed. This mixer is designed for a standard of 802.11 for use in Wi-Fi communications. The linearization technique for the third-order transconductance (g_{m3}) cancellation with modified derivative superposition (MDS) is utilized to enhance the linearity performance of the proposed mixer. The MDS technique employs an auxiliary PMOS transistor in parallel with the NMOS transistor in the lower tree (transconductance stage) for reducing the third-order intermodulation distortion (IMD3). Besides, a switched buffer stage and the active loads are employed to improve the conversion gain of the mixer. High gain and high linear mixer is designed by the MDS technique and switched buffer. The proposed mixer is analyzed, and simulated using a 0.18 µm CMOS TSMC process; The LNA achieves 9.1dB conversion gain, maximum input third-order intercept point (IIP3) of +15dBm, double side-band noise figure (DSB NF) of 15.6 dB. This module consumes 2.06 mW DC power from a 1.2 V power supply in the RF frequency of 10 GHz.

Keywords: CMOS, Linearity, Low voltage mixer, Conversion gain, Switched buffer

1. Introduction

The ultra-wideband (UWB) systems are generally used in wireless local area networks (WLAN) with a small distance and high data rates. The multi-band orthogonal frequency division multiplexing (MB-OFDM) UWB system uses a particular band of frequency (3.1-5GHz or 3.1-10.6GHz) to data access [1-3]. The standard of the IEEE 802.15.3a UWB system is recently allowing for MB-OFDM and direct-sequence code-division multiple-access as candidates for wireless personal area networks (WPAN) standards. Based on the specification of MB-OFDM, the band of UWB is separated into 14 frequency bands; each of them has a 528 MHz bandwidth. In some systems, each 528MHz frequency (of 14 bands) is consists of 128 channels, each of them has 4.125 MHz bandwidth [3]. The standard of 802.11 provides numerous different radio frequency ranges for use in Wi-Fi communications. Each range is divided into a multitude of channels. In the standards, channels are numbered at 5 MHz spacing bands. Also, in some literature, it has been recommended that the UMTS bands should be paired for UMTS FDD deployment with frequency blocks in multiples of 5 MHz [1-5]. The focus of this research is the design and analysis of a direct-conversion mixer with high linearity and high gain for a UWB receiver. In the architecture of direct-conversion circuit and system design, the technology of CMOS can present a single-chip solution which seriously decreases the area and cost; this is extensively used in the designing of UWB transceivers [4]. In the design of the analog front-end scheme, the receiver linearity is dominated by low noise amplifiers (LNAs) and mixers; consequently, the dynamic range (DR) of the receiver is always restricted with the primary mixer. So, the first mixer plays a significant role in deciding the linearity of the overall system [5].

The CMOS technology scaling facilitates the successful design of low power dissipation, high gain, and low noise CMOS RF front-end [6]. However, by the development of the device technology, the linearity has not benefited, which has motivated numerous methods of linearization. In [7], a method of derivative superposition (DS) is employed; it utilizes an auxiliary p-channel metal oxide semiconductor (PMOS) transistor to neutralize the nonlinear effect of primary N-channel metal oxide semiconductor transistor (NMOS) and to enhance the performance of IIP_3. To achieve these purposes, the transistor PMOS is operated in the weak inversion region, with positive third-order transconductance (g_{m3}), whereas the NMOS transistor, with negative g_{m3}, is adjusted at moderate inversion. So, the total g_{m3} in the differential output of the mixer will be close to zero [7]; details are given in section 3. Also, in this paper, the switched-buffer is established to enhance the conversion gain in the output of the mixer. Besides, this will reduce the power consumption, and designing the circuit with low voltage makes it possible.

In this paper, a UWB down-converting active CMOS mixer is presented with a Gilbert-cell structure with a new topology in the stage of transconductance to enhance the IIP3 of the mixer with a new topology in the output of the mixer with buffer stage to improve the output swing. The other sections of this paper are structured as follows. In Section 2, the paper analyzes the mixer in detail and compares it with a conventional famous switching mixer with double balanced (Gilbert cell), and the small voltage mixer using a switched buffer. Section 3 provides a high-linearity mixer for the down-conversion system. In section 4, simulation results and comparison with other works will be presented; and finally the conclusion section is presented in Section 5.

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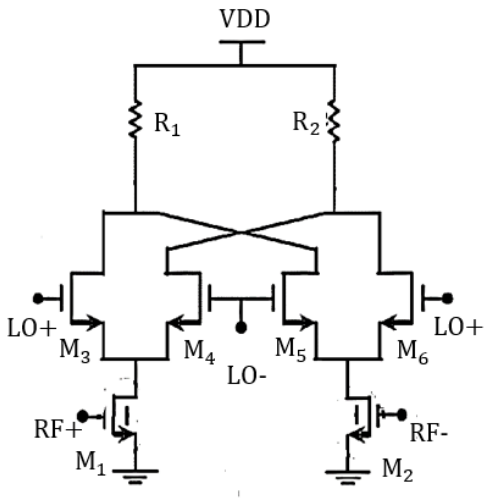


Figure 1 CMOS Gilbert-cell mixer (GmSw)

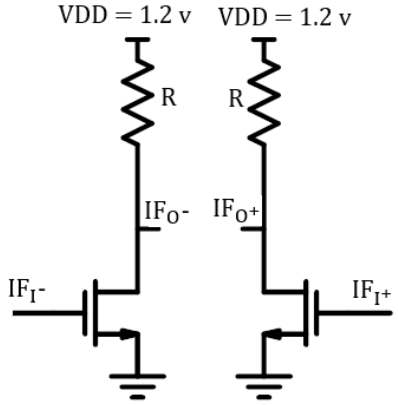


Figure 2 The traditional buffer with load (R)

2. Conventional gilbert mixers and the optimized mixer

Because of excellent isolation of LO port to RF port, and LO to IF port, which solves the problem of DC offset, the conventional double-balanced Gilbert-cell mixer is selected for our research [4, 5]. Figure 1 illustrates the CMOS Gilbert mixer (GmSw) with double balanced; it consists of switch stages, transconductance parts, and the output loads [8]. The structure of the dual-balanced Gilbert mixer is more linear than the switching mixer with a single balanced structure. Transistors ($M_1 - M_6$) are designed to work in the saturation region, to achieve high conversion gain and good linearity. A local oscillation signal (V_{LO}) drives the upper tree transistors (switch stages). The power of local oscillation must be great sufficient to create the transistors ($M_3 - M_6$) work as switches. The mixer performs like a multiplier to sample the RF signals. The mixer's conversion gain can be expressed as:

$$\mathrm{G} \approx \frac{V_{IF}}{V_{RF}} = 20\log(\frac{2}{\pi}\, g_m R_L) \tag{1}$$

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_G - V_{TH}) \tag{2}$$

$$\mathrm{G} \approx 20\log[\frac{2}{\pi}\mu_n C_{ox} \frac{W}{L}(V_G - V_{TH})R_L] \tag{3}$$

where C_{ox} is the oxide capacitance of MOSFET, μ_n is the mobility of electrons in silicon surface, L and W are the effective gate length and the gate width, respectively. R_L is represented as the impedance of load, and g_m represented the conductance of M_1 and M_2. Suppose that LO is expected with a waveform of sinusoidal, the value of gain (C.G) be able to attain as [9]

$$\mathrm{G} \approx 20\log[\frac{2}{\pi} g_m R_L \left(1 - \frac{\sqrt{2}(V_G - V_{TH})_{SW}}{\pi V_{LO}}\right)] \tag{4}$$

where $(V_G - V_{TH})_{SW}$ corresponds to the over-drive voltage of $M_3 - M_6$. V_{LO} is the amplitude of the LO signal. While the supply voltage is under 1.2 V, the stages (M_1–M_2) are worked in the triode region.

In the reference [9], conventional Gilbert-cell switched transconductor mixer (SwGm) with double-balanced structure is described. The transconductance stages are considered in the region that the transistors operate in the saturation region. Also, the switch stage is considered in a condition that the transistors work in the triode mode, while the supply voltage is small [10].

Comparing the GmSw and SwGm demonstrated that, the Gilbert-cell switching transconductance mixer (SwGm) is worse than the (GmSw) mixer with Gilbert-cell structure according to the conversion gain. Moreover, the bias current directly affects the conversion gain causing a significant voltage reduction in load [4]. Consequently, it decreases the voltage swing headroom. The selection of load (R_L) will change the output swing and the conversion gain. Moreover, by this technique, we cannot achieve the high linearity for a mixer. Therefore, to overcome these problems, a new optimization technique is required.

2.1 Switched buffer

Figure 2 illustrates the conventional buffer. In this figure (IF_i-) and (IF_i +) are the input signals and (IF_o-) and (IF_o +) are the conventional buffer's output signals with the output load of (R). Also, Figure 3 shows the simulated output signals of IF_i+, IF_o+, IF_i-, and IF_o-, respectively. Figure 3(e) demonstrates differential output signal ((IF_o+) - (IF_O-)) of the traditional buffer.

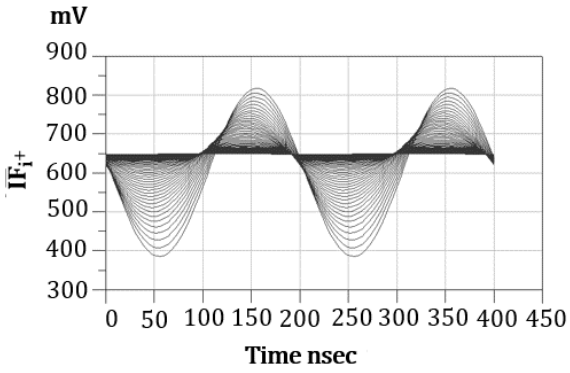
To improve the output voltage swing, the proposed switched buffer is used; as illustrated in Figure 4, ((IF)(o(SwB))-) and ((IF))_(o(SwB))+) are signals of the proposed switched buffer output. The sizes of the NMOS and PMOS transistors in Figure 4 are 45μm/o.18μm, and 90μm/0.18μm, respectively. Figure 5 defines the differential signal ((IFoSwB+) - (IFOSwB-)) of the designed switched buffer.

As illustrated in Figure 3(e) and Figure 5, the total voltage of the designed switched buffer is about 3.5 degrees better than the voltage of the conventional buffer. Additionally, the recommended circuit is achieved high conversion gain; also it decreases the amount of power supply, and therefore low power dissipation is attained.

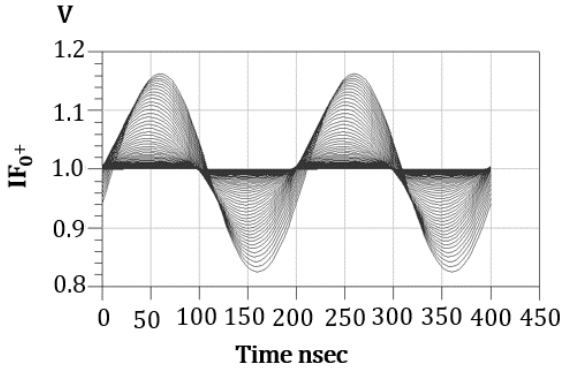
3. Linearity analysis of the designed mixer

In nanoscale MOSFET design, the linearity of the modules degrades because of bias supply voltage decrease and effects of high-field mobility. The linearity of the mixer is an essential factor due to the cross-modulation distortion in mixer design. In particular, the linearity of the receiver becomes a critical issue. Typically, in the design of analog front-end circuits, while the dynamic range (DR) of receiver is restricted by the primary mixer, so the receiver's linearity is dominated with a module of mixer. Therefore, a mixer with high linearity and high input third-order intercept point (IIP3) is preferred to further improve the signal to noise ratio (SNR) of the RF output signal [11-13]. A few linearization methods have been recommended and published for the RF mixer purposes [13-15].

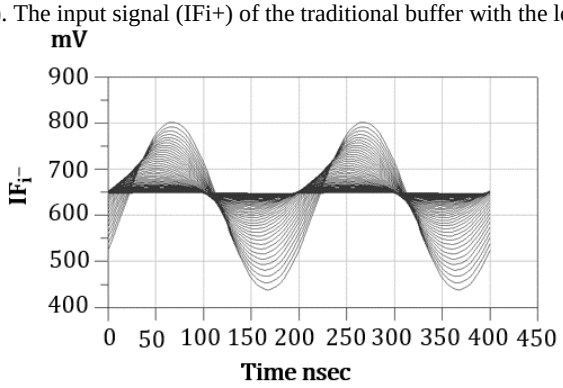
In this paper, a new linearization technique using a third-order transconductance (g_{m3}) elimination technique in the differential output of the mixer is proposed. In this technique, an additional PMOS transistor is applied to the transconductance



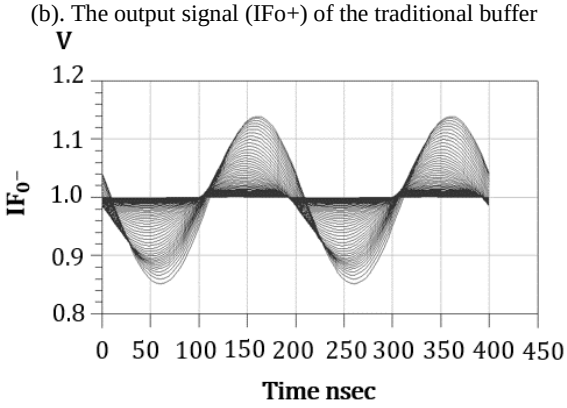
(a). The input signal (IFi+) of the traditional buffer with the load



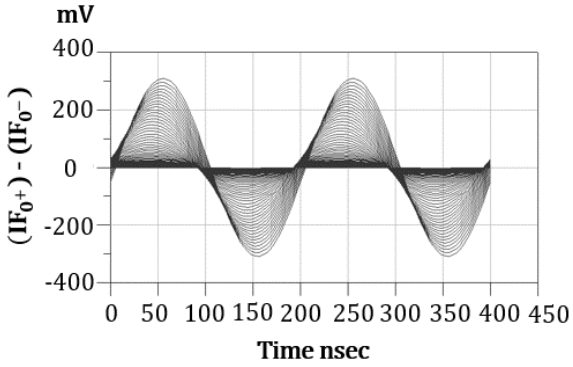
(b). The output signal (IFo+) of the traditional buffer



(c). The input signal (IF_i-) of the traditional buffer



(d). The output signal (IF_o-) of the traditional buffer with the load



(e). The differential output signal ((IFo+) - (IFO-)) of the traditional buffer

Figure 3 Output signals of the traditional buffer

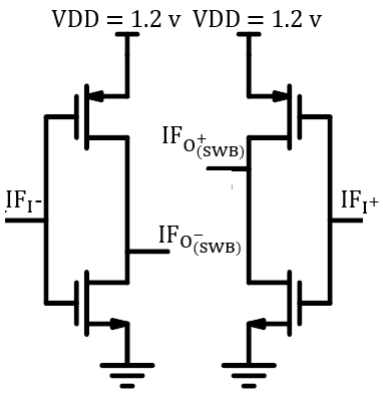


Figure 4 The recommended switched buffer

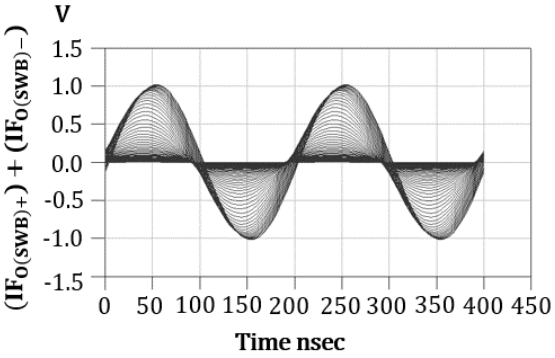


Figure 5 The differential output signal ((IFoSwB+)-(IFOSwB-)) of the switched buffer

part in parallel with the NMOS transistor for reducing the intermodulation distortion of the third-order (IMD3) and improving the IIP3. The transistors with g_{mn3} (third-order transconductance of NMOS transistor) and g_{mp3} (third-order transconductance of PMOS transistor) are combined in the differential output of the mixer get a flat g_{m3} region, and made g_{m3} total near zero in some region. To implement this approach, g_{mn3} and g_{mp3} must be adjusted with bias voltage, somehow

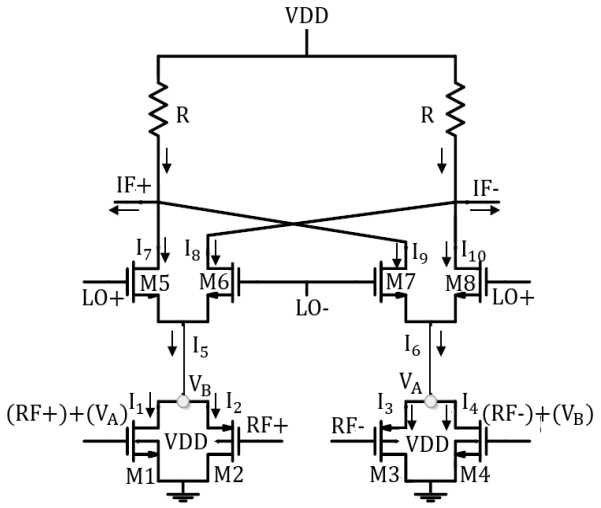


Figure 6 Circuit of the recommended high-linearity RF mixer

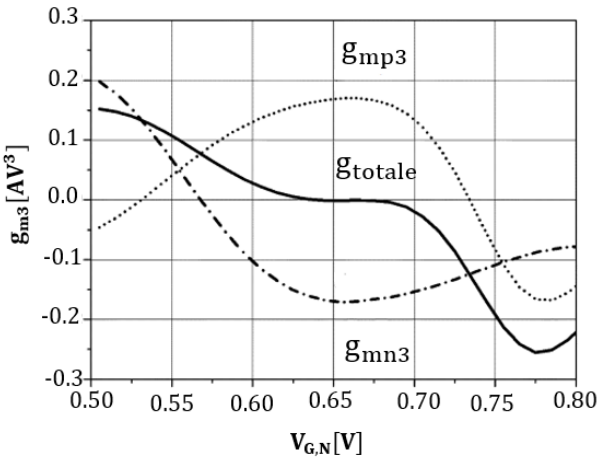


Figure 7 Simulated g_{total} compensation results of two connected in parallel transistors (NMOS and PMOS)

that in the operation region, the total g_{m3} of the parallel connection of FETs will be near zero.

The drain-source current (i_{DS}) of a common source (C.S) NMOS transistor can be indicated by using a Taylor series expansion as follows:

$$i_{DS} = I_{dc} + g_{mn1}v_{gs} + \frac{g_{mn2}}{2!}^2 v_{gs}^2 + \frac{g_{mn3}}{3!}^3 v_{gs}^3 + \quad (5)$$

Where $g_{mn}^{(n)}$ explains the nth-order transconductance of NMOST transistor, and v_{gs} is the gate to source voltage of NMOS transistors. Also, the drain-source current (i_{DS}) of PMOS transistor can be explained using an expansion of Taylor series:

$$i_{DS} = I_{dc} + g_{mp1}v_{sg} + \frac{g_{mp2}}{2!}^2 v_{sg}^2 + \frac{g_{mp3}}{3!}^3 v_{sg}^3 + \quad (6)$$

Where $g_{mp}^{(n)}$ explains the nth-order transconductance of PMOS transistor, and v_{sg} is the source-gate voltage of PMOS transistors. The g_{m3} plays a significant role in the IMD3. The idea of IMD3 cancellation is easy, but it's realization is not simple, because of the complexity of splitting the IMD3 and fundamental signal. Now, we explain that an extra folded-cascode PMOS transistor can be like an IMD sinker. Figure 6. Illustrates the recommended circuit with two auxiliary PMOS transistor.

The resulting output current i_{total}, in Figure 6, can be explained as the differential of i_{IF+} andi_{IF-}. In Figure 6, it can be supposed that, the signal of LO is a square wave and the signal of RF is a sinusoidal wave $v_{RF}^{+}_{-} = V_{RF}\sin\omega_{RF}t$. The i_{total} multiplied by a current of an ideal square wave (I_{LO}). In the first half cycle, when the LO+ signal is positive, LO- signal is negative; M_5 and M8 are on, while M_6 and M7 are off. Thus, the currents of i_{total} and i_{IF+} and i_{IF-} can be expressed as:

$$I_1 = I_{dc} + g_{mn1}v_{gsn1} + \frac{g_{mn2}}{2!}^2 v_{gsn1}^2 + \frac{g_{mn3}}{3!}^3 v_{gsn1}^3 + \quad (7)$$

$$I_2 = I_{dc} + g_{mp1}v_{sgp1} + \frac{g_{mp2}}{2!}^2 v_{sgp1}^2 + \frac{g_{mp3}}{3!}^3 v_{sgp1}^3 + \quad (8)$$

and $v_{gsn1} = v_{sgp2} = v_{RF+}$ and $v_{sgp3} = v_{RF-}$,
and $v_{RF+} = -v_{RF-} = v_{sgp3}$ (9)

equation can be explained as follows:

$$I_3 = I_{dc} + g_{mp1}v_{gsn1} + \frac{g_{mp2}}{2!}^2 v_{gsn1}^2 - \frac{g_{mp3}}{3!}^3 v_{gsn1}^3 +$$
and $I_5 = I_1, I_6 = I_3$ (10)

$I_7 = I_5 \times I_L$ or $I_7 = I_1 \times I_L$
and $I_{10} = I_6 \times I_L$ or $I_{10} = I_3 \times I_L$ (11)

$I_{IF+} = I_R - I_7$, $I_{IF-} = I_R - I_{10}$ and i_{total} is defined the differential output signal ($I_{IF+} - I_{IF\_}$), thus $i_{total} = I_{IF+} - I_{IF\_} = I_{10} - I_7$ or $i_{total} = -(I_7 - I_{10})$ and thus, by using equations (7) and (10), $(I_7 - I_{10})$ can be estimated by

$$(I_7 - I_{10}) = (I_1 - I_3) \times I_L = (I_{dc} + g_{mn1}v_{gsn1} + \frac{g_{mn2}}{2!}^2 v_{gsn1}^2 + \frac{g_{mn3}}{3!}^3 v_{gsn1}^3 +) - (I_{dc} + g_{mp1}v_{gsn1} + \frac{g_{mp2}}{2!}^2 v_{gsn1}^2 - \frac{g_{mp3}}{3!}^3 v_{gsn1}^3 +) = (g_{mn1} - g_{mp1})v_{gsn1} + (g_{mn2} - g_{mp2})^2 v_{gsn1}^2 + (g_{mn3} - g_{mp3})^3 v_{gsn1}^3 + \ldots \quad (12)$$

where $g_{mn}^{(n)}$ expresses the nth-order trans conductance of NMOS, v_{gsn1} the gate-to-source voltage of NMOS transistor (M_1), and $g_{mp}^{(n)}$ expresses the nth-order transconductance of PMOS (M_3). g_{mn3} and g_{mp3} are negative at the strong inversion region for both NMOS and PMOS. The original transistor (NMOS) is biased in strong inversion, while the PMOS transistor as an auxiliary transistor is biased in the moderate inversion. Consequently, the third-order nonlinearity effect of two devices can be cancelled out (g_{m3}=$g_{m3(total)}$=g_{mn3}-g_{mp3}=0), and high linearity of IIP_3 can be achieved, as defined in Figure 7.

Therefore, by supposing that the drain is shorted at the signal frequency, the voltage amplitude of IP3 can be defined as [13]

$$IP3 = \sqrt{\frac{4}{3}\frac{g_{m1}}{g_{m3}}} = \sqrt{\frac{4}{3}\frac{g_{mn1} - g_{mp1}}{g_{mn3} - g_{mp3}}} \quad (13)$$

From (13) it's obvious that, the IP3 of the mixer can be enhanced by degradation of g_{m3} efficiently. The complete diagram of the recommended mixer with linearization technique and the switched buffer is demonstrated in Figure 8. The proposed circuits for linearity improvement and voltage swing are appropriated to a Gilbert-cell structure, as shown in Figure 8. The transconductor stage (M_1-M_4) converts the input RF voltage signals into small output current signals to the commutating stage. The commutating stage is usually driven with the LO signal of the RF front-end stage. The switching stage (includes M_5–M_8) operates as perfect switches, while the power of LO port is big. In small power of LO, the switching module operates as a small signal amplifier.

Table 1 Performances of CMOS UWB mixers

Ref.	Process CMOS (μm)	LO power (dBm)	Gain (dB)	Freq. (GHz)	IF (MHz)	IIP3 (dBm)	NF(dB)	Supply V	area
[17]	0.18	-1	9.5-12.5	0.3-25	10	-	-	4.9	Mid
[10]	0.13	5	5-2	9-50	10	-	-	3.3	Low
[18]	0.18	-2	5.5	0.2-16	528	-	-	1.8	Mid
[19]	0.18	9	5.2-2.5	3-8.72	528	5	6.8-7.3 (DSB)	1.8	High
[20]	0.18	3	11.5-13.5	2-27	10	0	14.3-17(DSB)	2	High
[21]	0.18	5	5.7-4.3	0.5-7.5	100	-5.7	15	0.77	Mid
[22]	0.13	13	-3-1	10-35	100	-	-	1.6	Mid
[4]	0.18	0	7.2-4.3	3.4-6.8	10	2-3	13.9-14.4(DSB)	1	High
This work	0.18	0	9	8-10	5	+15	15.6	1.2	high

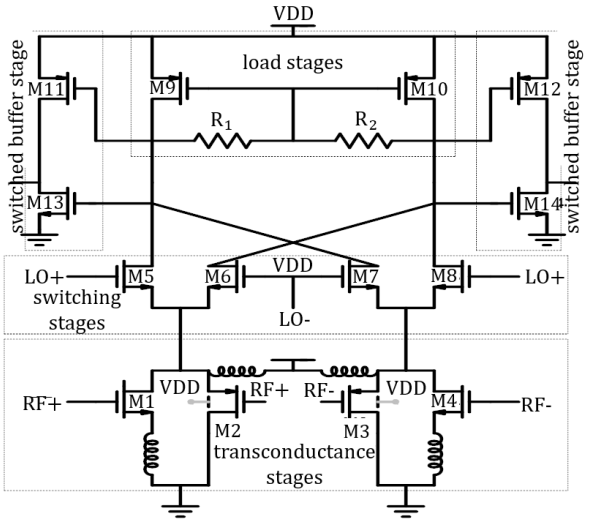


Figure 8 The complete schematic of the proposed mixer

The transistors of the mixer are biased between the saturation region and triode to construct transistors M_5–M_8 perform as ideal switches with lower driven power. The RF signal is inserted from the source of M_5–M_8, so down conversion to the IF signal is produced by the switching stage with the multiplier function. The ratio of the Transistors and the DC operation point will affect the necessity of the LO signal. The output stage consists of M_9, M_{10}, R_1, and R_2, which transforms the current signal to the voltage. The transistors M_9 and M_{10} can supply suitable swing of voltage headroom. The transistors M_{11}, M_{13} and M_{12}, M_{14} act as a stage of switched buffer to obtain the impedance matching to 50-Ω.

The mixer's conversion gain without auxiliary transistors (without M2 and M3 as PMOS transistor for linearity improvement) can be explained as:

$$G \approx \frac{V_{IF}}{V_{RF}} = 20\log[(\frac{2}{\pi}\ g_m R_L)(g_{mO}(r_{on}\| r_{op}))] \quad (14)$$

where g_{mo} is the transconductance of the output transistors, R_L is the impedance of input port (in buffer), r_{on} is the drain-source resistance of N-channel MOS transistor, and r_{op} is the drain-source resistance of P-channel MOS transistor.

4. Simulation results of designed mixer

As illustrated in Figure 8, the suggested mixer has four major stages: transconductance stages (M_1-M_4), switching stages (M_5-M_8), active load (M_9-M_{10}) with R_1 and R_2, and output switched buffer stage (M_{11}, M_{13} and M_{12}, M_{14}). In order to decrease the power consumption and power supply, resistive loads are changed with active PMOS in the output switched buffer stage; it also provides the possibility to improve the conversion gain without giving up the voltage swing headroom.

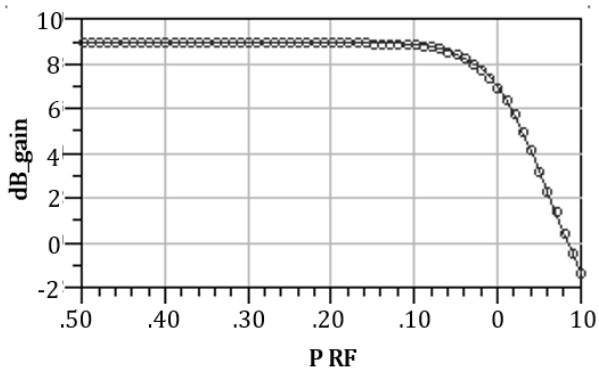


Figure 9 Simulated C.G versus the power of RF signal with 0 dBm LO power and 5 MHz IF frequency

The sizes of devices in Figure 8 are $(W/L)_{M1,4}$ = 30μm/0.18μm, $(W/L)_{M2,3}$ = 70μm/0.18μm, $(W/L)_{M5\text{-}8}$ = 90μm/0.18μm, $(W/L)_{M9,10}$ = 200μm/0.18μm, $(W/L)_{M11,12}$ = 90μm/0.18μm, and $(W/L)_{M13,14}$ = 45μm/0.18μm.

The recommended high gain, low voltage, and low power UWB down-conversion mixer with high linearity is designed and analyzed in a 1P6M 0.18μm CMOS technology. The frequency of LO and RF were swept at 10 GHz with a 5 MHz IF frequencies. The output buffer consumes 0.4 mW of power from a 1.2 V of power supply. The total DC power consumption of the designed circuit, including output buffers, is 2.06 mW; this module consumes a current of 1.72 mA from a 1.2 V of power supply.

High gain and high linear design is the main improvement of the recommended mixer. Figure 9 shows the simulation results of gain (C.G) versus the power of the RF signal.

Figure 10 denotes the simulation result of gain compression point (P_{1-dB}) for the proposed mixer versus the RF power. As illustrated in this figure, the $P_{1\text{-}dB}$ of 2.5 dBm is attained.

Figure 11 illustrates the resulted output power of fundamental and third-order intermodulation (IM3) vs. the RF input at the output of the switched buffer. By supposing that spacing and channel bandwidth are both 40 kHz, with the proposed linearization technique using the g_{m3} cancellation technique in the output of the module, the IIP3 is obtained 15 dBm at 10 GHz. The simulation of DSB noise figure (NF) shows that, the minimum noise figure for 10 GHz is 15.6 dB, as demonstrated in Figure 12.

Table 1 summarizes the output results of the proposed mixer with comparison to the previous wideband mixers. As shown in [16], it requires high power consumption with a large supply voltage of 4.9 V. As illustrated in [16-19], Gilbert mixer (GmSw) with the voltage supply of under 1 V is hardly satisfied. References [18, 19-22] need an LO signal with high power.

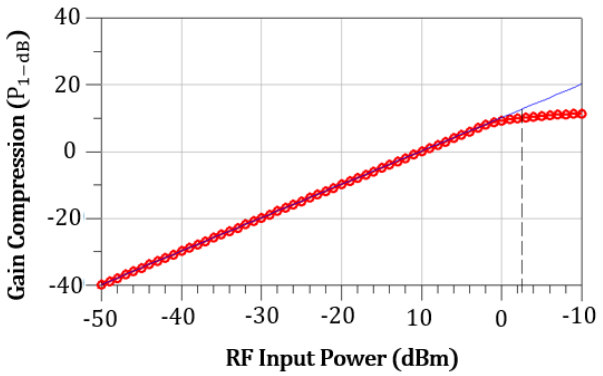


Figure 10 The simulated 1-dB compression point ($P_{1-\mathrm{dB}}$) versus the RF power

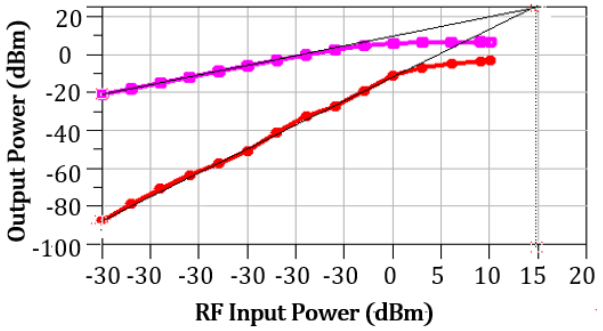


Figure 11 Simulated IIP3 at 10 GHz

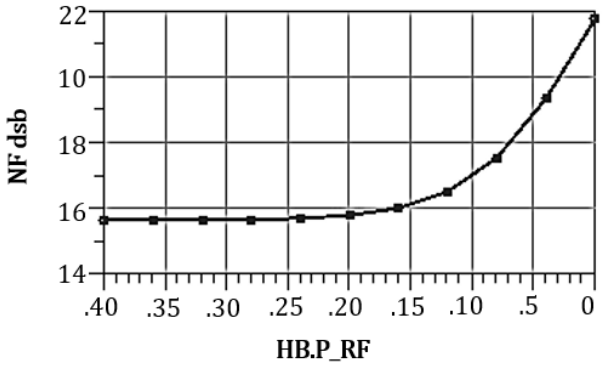


Figure 12 Noise figure of DSB versus the RF frequency with-40 dBm RF power and 0 dBm LO power

Reference [20] reported just the power dissipation of the core mixer, without the output buffer. The Gilbert mixer (GmSw) and the mixers with distributed configuration could not attain the requirement of the receiver, while the voltage supply is small than 1 V.

The bulk-pumped mixers [21, 22] can attain little power dissipation, but need a large power LO signal. The recommended mixer in [4] has a small power consumption of 2.9 mW with the 1 V supply voltage, but it has high power consumption and low IP3 compared to this work. Besides, in comparison with previously reported papers, the recommended mixer dissipates a current of 1.72 mA from a supply of 1.2 V, a relatively small DC power of 2.06 mW, and with very high IIP3 of 15 dBm; but the proposed mixer occupies high silicon area. As illustrated in Table 1, compared with the achieved results, the recommended module is suitable and most appropriate for RF module applications.

5. Conclusion

A 1.2 V low current consumption, equal to 1.72 mA, low power consumption equal to 2.06 mW, and high-linearity of 15 dBm with IF equal to 5 MHz UWB Gilbert mixer topology has been presented with a new switched buffer topology with a new g_{m3} cancellation technique. The recommended technique is easily appropriated to tmicrowave and RF designs; besides, the linearity performance of the circuits can be highly enhanced with no consuming additional power dissipation. The recommended mixer is appropriate for wideband system purposes. These techniques will be employed for any other radio frequency modules, such as power amplifier and LNA in the receiver, for further improve the conversion gain, linearity, and decrease the power supply and power consumption.

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