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Design of power efficient, high-speed 4-bit comparator in UMC 180 nm technology

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Abstract

Power, Area, and Delay are the three important performance metrics used for analyzing any digital circuit. This paper explores different digital circuit design styles to achieve a better trade-off between the performance metrics. 4-bit Comparator based on 2's complement addition principle is designed and implemented using these different digital circuit principles. Full adder and the other components required to implement 4-bit comparator are designed and implemented using Majority Gate Logic (MGL), Mirror Adder Logic (MAL), Complementary Pass Transistor Logic (CPL), Transmission Gate Logic (TGL) and Gate Diffusion Input Logic (GDI) for studying their performance under different stringent conditions of Temperature, Power supply, etc. The circuits are realized in the UMC 180 nm process using the Cadence Spectre Simulator with a power supply of 1.8 V.

Keywords: Power, Comparator, Performance metrics, Gate diffusion input logic

1. Introduction

Recent advances in the field of electronics made an enormous increase in the usage of portable electronic systems. In such types of portable applications, power dissipation has one of the most important design considerations making it to be vital for many researchers in the field of integrated circuit design. The concern about reducing the power dissipation has been increased with the scaling down of VLSI technologies. The number of transistors or gates per given chip area is increasing while the switching energy is not decreasing at the same speed and hence the power dissipation increases making the removal of accumulated heat more difficult and expensive. To overcome this limitation various design approaches at different levels of abstraction that include circuit, architectural, or system have been proposed in various existing works of literature.

Power dissipation in any digital circuit has three major contributions Dynamic Power-Indicates loss of energy in charging and discharging of output capacitance while switching the output states, Static Power- Usually termed as leakage power determined by the total leakage current of the circuit under steady-state conditions and Short Circuit power- Because of current flowing through the input source to the ground during short circuit conditions. Most of the design approaches are meant for reducing the dynamic power dissipation as it contributes largely to the total power dissipation. In the existing literature, various digital logic techniques like Majority Gate Logic (MGL), Mirror Adder Logic (MAL), Complementary Pass Transistor Logic (CPL), Transmission Gate Logic (TGL) and Gate Diffusion Input Logic (GDI), etc are discussed to achieve the required performance.

In the present day high-performance systems like real-time Digital signal processors, Microcontroller based systems consist of high-speed circuits that include ADCs, Filters, etc which require arithmetic and logic operations that should be executed at very high speeds at the cost of low power. Digital comparator is one such ALU block that has wide applications in the data processing, encryption applications and more specifically decoding instructions given to a microprocessor-based system or decision-based control system. Several architectures have derived in the works of literature for implementing a 2-bit or 4-bit comparator. In [1], a 2-bit comparator is implemented using all-n-transistor (ANT) dynamic CMOS logic based on the tree structure. A comparator based on bit-wise competition logic is proposed in [2]. A low power-based style has been used to design a comparator in [3]. [4] Proposes a 2-bit comparator based on reversible logic. In [5], 45 nm and 90 nm technologies are used for designing a comparator in different logic styles. Various high-speed comparator architectures have been discussed in [6]. [7] Describes a comparator based on multiplexer architecture with a single clock operation. [8] and [9] describes various static circuit design styles targeted to achieve low power digital circuits with countable speeds.

This paper presents the performance of different static logic styles to achieve low power consumption and high packing density by designing a 4-bit comparator based on 2's complement addition and the circuits are realized in UMC 180 nm process using the Cadence Spectre Simulator with a power supply of 1.8 V.

The proposed architecture of a 4-bit comparator based on 2's complement addition is discussed in section 2. While section 3 describes the architecture of Full-Adder associated with the proposed architecture using different logic styles. Simulation results and the conclusions are presented in section 4 and section 5 respectively.

2. Architecture of 4-bit comparator

Various comparator architectures are discussed in the existing literature for different speeds, power, and circuit

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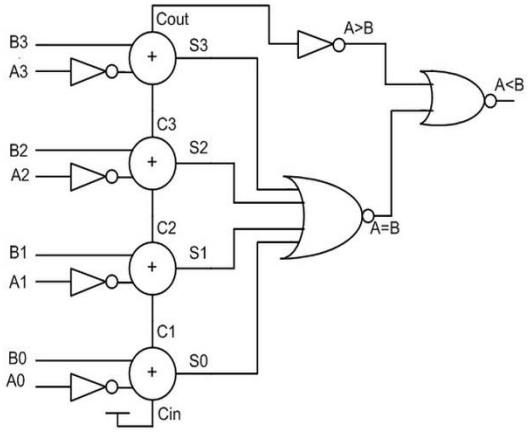

Figure 1 Architecture of 4-Bit Magnitude Comparator

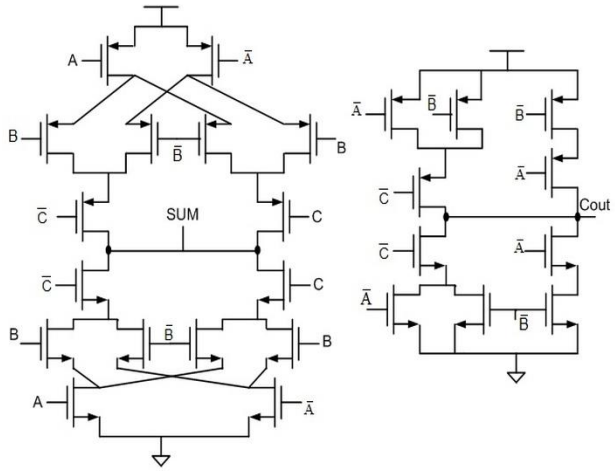

Figure 2 FA Architecture using Majority Gate Logic (MGL).

complexity. The basic need of comparator is to find the arithmetic relation between two variables (say A, B) in terms of either lesser than or greater than or equal to. The traditional method of comparison is the finding of relative magnitudes of the variables. One of the most common approaches to find arithmetic relation is based on a bit-wise comparison for digital variables. In which Most Significant Bits (MSB) are compared and if the relationship is found between these bits than that is the output of comparator else if these two MSB bits found to be equal, then the comparison result depends on lower-order bits. The bit-wise comparison continues until all the bits of two variables are compared until a relation is found. Since the comparison is bit-wise, it requires more logic gates in-turn transistors and hence results in larger power dissipation and longer delays.

To overcome the circuit design complexity in terms of the number of transistors, the power consumed and smaller delays, a new method of magnitude comparison is proposed. The basic principle of proposed logic is based on 2's complement addition. To find the arithmetic relation between two variables (say A, B), bit-wise (B-A) subtraction is performed using 2's complement logic. As per the 2's complement addition, if the addition operation results in a carry than the relation is A ≤ B, if all the sum bits are Zero than the relation is A = B and while if carry don't exist and if all the sum bits are not Zero than the relation is A > B. The architecture based on this principle for the comparison of two 4-bit inputs (Say, A [3:0] and B [3:0]) is shown in Figure 1.

From the Figure 1, it can be observed that to perform (B-A), A is bit-wise complemented using Inverters and applied as the second input to full adders (FAs), while the first stage full adder is applied with '1' at Cin to convert input 'A' into twos complement number. To study the performance metrics of different digital design techniques, full adder of Figure 1 used in developing the 4-bit comparator is designed using five design styles namely Majority Gate Logic (MGL), Transmission Gate Logic (TGL), Mirror Adder Logic (MAL), Complementary Pass Transistor Logic (CPL), and Gate Diffusion Input Logic (GDI) and is discussed.

3. Architectures of full adders (FAs)

The full adder plays a crucial role in designing the digital circuits that perform various arithmetic operations like addition, subtraction, multiplication, etc. It is so-called because it adds two binary digits and a carry-in coming from the lower order stages to produce Sum and Carry-out. Being the most critical part of digital circuits involved with multiple operations, which determines the comprehensive performance of the digital system. Hence designing the FA with less power and the acceptable delay has been the designer's challenge in the field of VLSI.

Full adder consists of three inputs- two inputs (Say, X, Y) which are externally applied, and one carry-in (Say Cin) input coming from the lower order stages producing two outputs- Sum (Say SUM), representing the addition result of two bits and Carry-Out (Say C_{out}), which acts as C_{in} for higher-order stages. The operating principle of a full adder is defined by two Boolean expressions representing each for two outputs and is expressed as,

$$\mathrm{SUM} = \sum \mathrm{m}(1, 2, 4\ 7) = \mathrm{A} \oplus \mathrm{B} \oplus \mathrm{C_{in}} \tag{1}$$

$$\mathrm{C_{out}} = \sum \mathrm{m}(3, 5, 6, 7) = \mathrm{A} \cdot \mathrm{B} + \mathrm{C_{in}} \cdot \mathrm{A} + \mathrm{C_{in}} \cdot \mathrm{B} \tag{2}$$

3.1 Full adder design using majority gate

From Eq. (1) and Eq. (2), the most straight forward approach for designing the adder is using logic gates like 3-input XOR gate for sum (SUM) output and 3-2 input AND gates with 1-3 input OR gate for Carry-out (C_{out}). From CMOS based circuit implementation of full adder modelled using Eq. (1) and Eq. (2), it is found that it requires 40-Transistors for producing SUM and C_{out} outputs. The transistors required to construct the FA can be reduced by modifying the SUM and C_{out} Boolean equations as follows,

$$\overline{\mathrm{SUM}} = \overline{\mathrm{A}} \cdot \overline{\mathrm{B}} \cdot \overline{\mathrm{C_{in}}} + \overline{\mathrm{A}} \cdot \mathrm{B} \cdot \mathrm{C_{in}} + \mathrm{A} \cdot \overline{\mathrm{B}} \cdot \mathrm{C_{in}} + \mathrm{A} \cdot \mathrm{B} \cdot \overline{\mathrm{C_{in}}} \tag{3}$$

$$C_{out} = \overline{\overline{\mathrm{A}} \cdot \overline{\mathrm{B}} + \overline{\mathrm{C_{in}}} \cdot (\overline{\mathrm{A}} + \overline{\mathrm{B}})} = MAJORITY\ (\mathrm{A}, \mathrm{B}, \mathrm{C_{in}}) \tag{4}$$

From the Eq. (2), it can be observed that the output Cout exists, whenever the majority of inputs exist and the same is shown in Eq. (4), termed as called "Majority Gate Equation", and hence the logic is called Majority Gate Logic (MGL). CMOS implementation of FA using Eq. (3) and Eq. (4) is illustrated in Figure 2.

From Figure 2, it can be observed that MGL implementation of FA requires a total of 32 Transistors out of which 6 for inverters, 10 for the majority gate i.e. for C_{out} and 16 for SUM output. Hence this logic requires 20 % less area compared to traditional CMOS implementation of FA based on Eq. (1) and (2).

3.2 Full adder design using mirror adder

The transistors count required for implementing FA based on Eq. (1) and (2) can be further reduced by reusing C_{out} for producing SUM. By applying Boolean algebraic rules, the SUM expression modelled using Eq. (1) can be factorized such that C_{out}

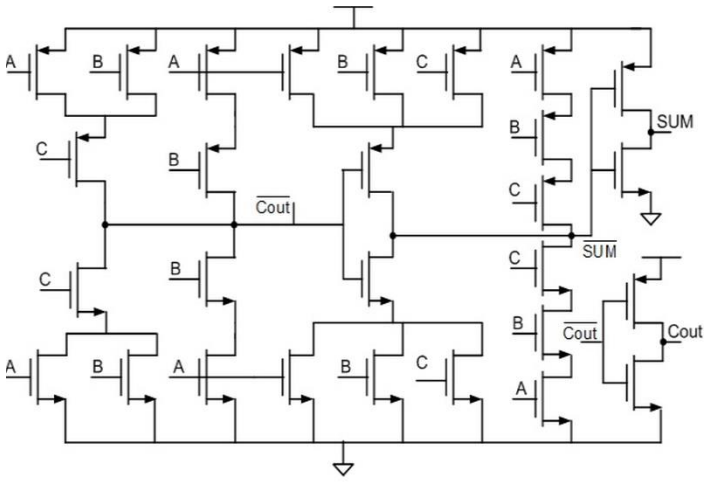

Figure 3 Full Adder design using Mirror Adder Logic (MAL)

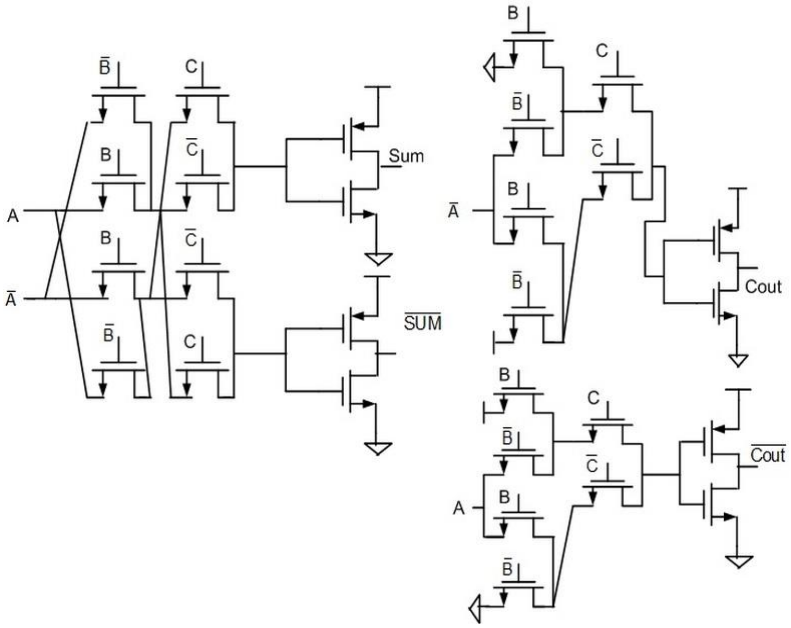

Figure 4 FA Architecture Using Complementary Pass Transistor Logic (CPL)

shown by Eq. (4) can be reused and thus the expression for SUM output is,

$$\mathrm{SUM} = \mathrm{A} \cdot \mathrm{B} \cdot \mathrm{Cin} + (\mathrm{A} + \mathrm{B} + \mathrm{Cin}) \cdot \overline{\mathrm{C_{out}}} \quad (5)$$

Figure 3 illustrates the CMOS implementation of FA based on Eq. (5) and Eq. (6). It can be inferred from the circuit implementation that the PMOS and NMOS network are alike rather than being the complement, unlike the traditional CMOS logic. This topology is termed as "Mirror Adder" and hence the logic is Mirror Adder Logic (MAL). The simplification involved here has reduced the number of series transistors resulted in uniform Layout. 28 transistors are utilized to implement the FA which is 30 % less compared to traditional CMOS logic and about 12.5 % less than MGL.

3.3 FA Using complementary pass transistor logic (CPL)

In contrast to static CMOS logic, Pass transistor logic offers greater lead in terms of three parameters area, power, and speed. Even though it provides better performance, it has been avoided in low power applications because of degraded logic voltage levels which result in reduced noise Margins. [10] Proposed an excellent method for utilizing the pass transistors which overcomes the disadvantages using static CMOS inverters and is termed as "Complementary Pass transistor logic (CPL)". In general, CPL consists of true and inverted variables; NMOS pass transistors and level shifter using inverters.

The full adder modelled using Complementary Pass transistor logic (CPL) is shown in Figure 4. CPL tries to reduce the number of transistors for implementing the FA logic by driving both gates together with source and drain terminals using the primary inputs unlike traditional CMOS logic [11]. It can be observed from Figure 4, that FA designed using the CPL [12] approach uses 30 Transistors in comparison to 40-Transistors based CMOS static logic [13].

3.4 Transmission gate logic (TGL) based full adder design

Unlike the digital gates, the Transmission Gate [14] is similar to a switch that operates in both directions. It consists of an NMOS and PMOS transistors connected in parallel and whose operation can be controlled by a control signal connected in complement to their respective gates. The FA modelled by Eq. (1) and Eq. (2) implemented using these transmission gates is illustrated in Figure 5. It can be noticed from Figure 5 that the

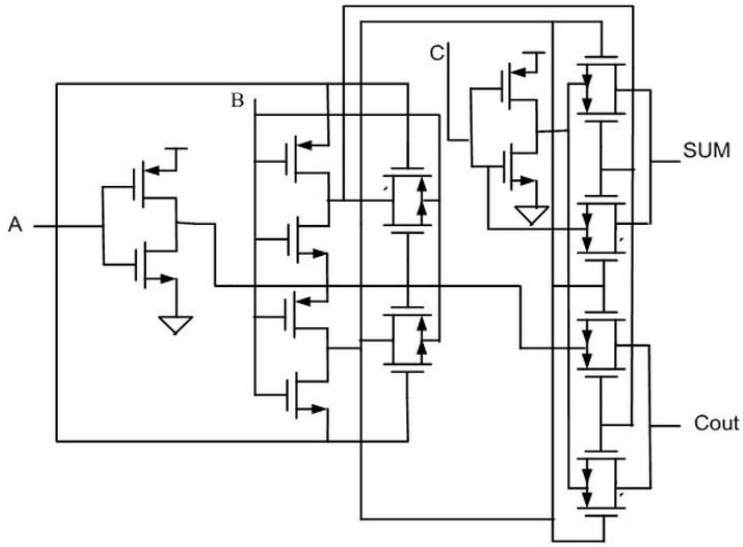

Figure 5 Full Adder design Using Transmission Gate Logic (TGL)

Table 1 Input Combinations for various Logic operations using GDI logic.

Function	G	P	N	Output
OR	A	B	'1'	A+B
AND	A	'0'	B	A.B
MUX	A	B	C	A'.B+A.C
XOR	A	B	B'	A'.B+A.B'
NOT	A	'1'	'0'	A'

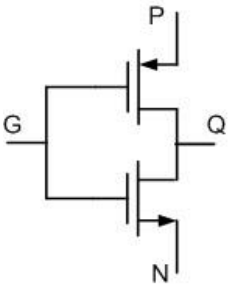

Figure 6 Basic GDI Logic Cell.

full adder implementation using transmission gate logic requires only 20-Transistors in contrast to 40 and 30-transistors in Static CMOS and CPL. Further, the use of transmission gates [15] allows to gain high speed and low power consumption in contrast to other logic styles and discussed in section 4.

3.5 Full adder design using gate diffusion input logic (GDI)

Gate diffusion input (GDI) logic is a power-efficient design technique that overcomes the various problems associated with the other static CMOS design styles. Using GDI, a wide range of logic circuits can be implemented by using only two transistors and suitable for fast and low power circuits with reduced transistor count compared to other existing CMOS design styles in the literature. The basic logic cell used in the GDI technique opted from [16] is reproduced here in Figure 6 for the sake of clarity. The logic cell resembles basic static CMOS inverter but with 4-terminals instead of two, 3-Inputs (Say G, P, and N) and 1-Output (Say Q) as shown in Figure 6.

Different logic operations can be implemented with GDI basic cell using various input combinations as presented in Table 1. The input combinations specified in Table 1 is based on the output equation of GDI cell and is expressed as,

$$Q = \overline{G} \cdot P + G \cdot N \quad (6)$$

To highlight the advantages of the GDI technique, Table 1 also presents the comparison of GDI and traditional CMOS logic implementation of various functions in terms of transistor count. It is evident from Table 1, that GDI logic uses a reduced number of transistors in contrast to the traditional CMOS circuit and hence results in low power dissipation and larger speed. Full adder (FA) using GDI has been implemented and illustrated in Figure 7 and can be observed that FA design using GDI logic requires a small transistor count in contrast to other logic styles [17].

4. Simulation results

In this work, the 4-bit Magnitude Comparator (MC) has been designed using five different design techniques that include Majority Gate Logic (MGL), Mirror Adder Logic (MAL), Complementary Pass Transistor Logic (CPL), Transmission Gate Logic (TGL) and Gate Diffusion Input Logic (GDI) [18]. The block diagram of a 4-bit magnitude comparator based on 2's complement addition using various GDI logic blocks is illustrated in Figure 8. The performance metrics of all the design techniques discussed are studied by designing and implementing 4-Bit comparator in 180 nm CMOS Process Technology [19] using Cadence Spectre environment at a supply voltage of 1.8 V. For the ease of implementation and for achieving optimized pull-up to pull- down ratios, the length and width of all the NMOS transistors are fixed at 500 nm and 1 µm respectively and 500 nm and 2.5 µm for PMOS respectively [20, 21, 23]. Table 2 shows the comparison of various logic techniques in terms of transistors for implementing the basic component full adder required in designing the proposed comparison technique using 2's complement addition. It can be perceived from Table 2, that GDI logic requires a very less number of transistors compared to other techniques.

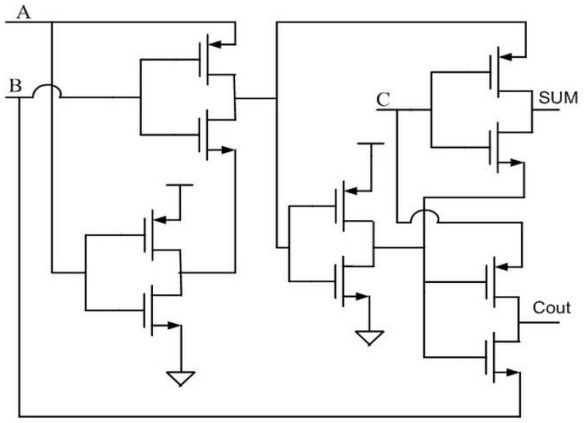

Figure 7 FA design using Gate Diffusion Input logic (GDI)

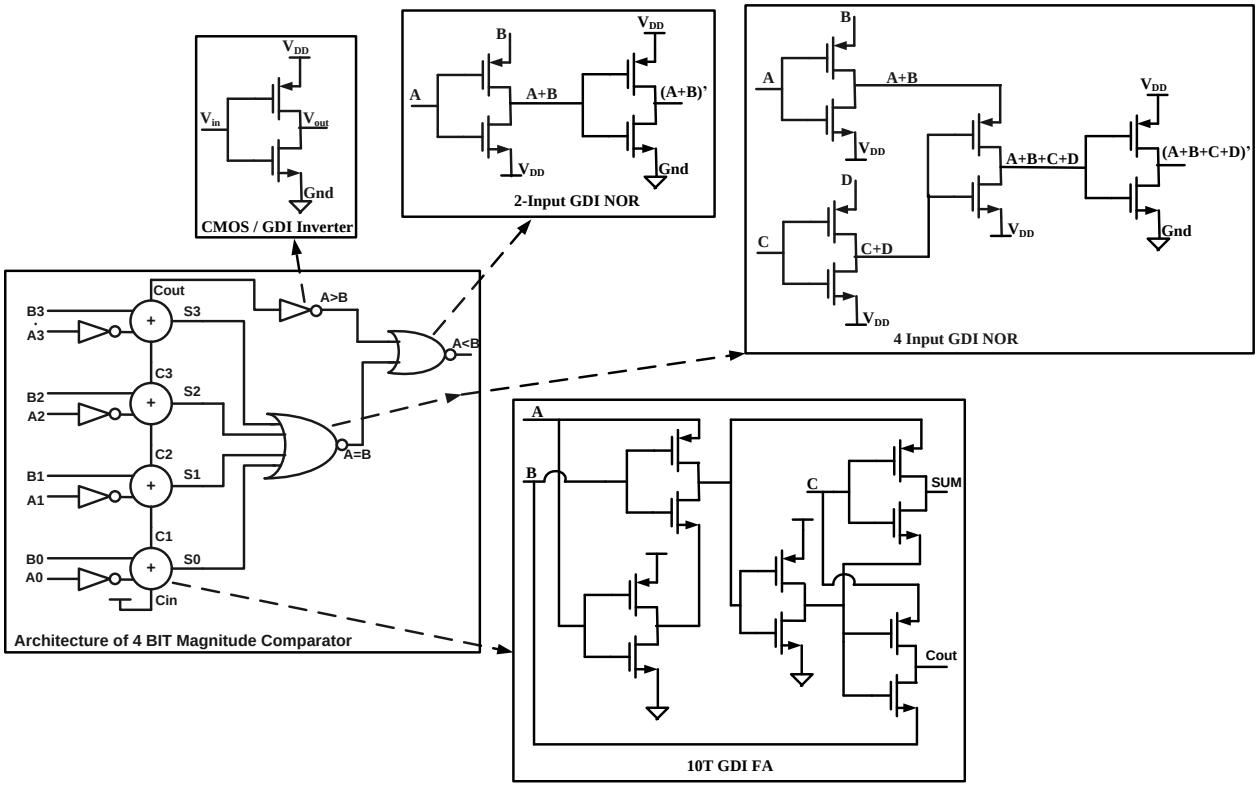

Figure 8 Architecture of 4 Bit Magnitude Comparator using GDI logic Blocks.

Table 2 Transistor count for various FA designs.

Sr. No	Design Style	Number of Transistors
1	MGL [8]	32
2	MAL [8]	28
3	CPL [12]	32
4	TGL [14]	20
5	Hybrid [22]	18
6	GDI	10

Figure 9 depicts the power variation of the 4-bit comparator depicted in Figure 1 concerning temperature. Figure 10 shows the power variations with respect to input voltages. It can be observed from Figure 9, that the power dissipation increases with temperature, and this variation found to be very small in GDI logic. From Figure 10, it can be inferred that the GDI exhibits less power dissipation compared to other logic styles.

Figure 11 illustrates the performance analysis of the 4-bit magnitude comparator designed using various design styles in terms of the number of transistors, power, and speed in terms of bar diagram, and the same is illustrated in Table 3. Figure 12 shows the simulation results of the 4-bit Comparator implemented using the GDI technique in the 180 nm process using the Cadence Spectre environment.

5. Conclusion

The performance metrics power, delay, and area of 5 different CMOS logic design styles are studied in this paper. 4-Bit comparator using 2's complement addition technique has

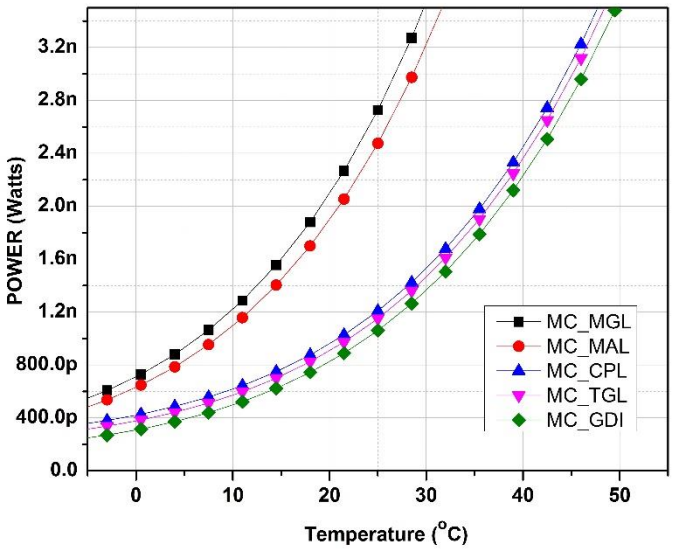

Figure 9 Variation of Power with Temperature of 4-bit MC

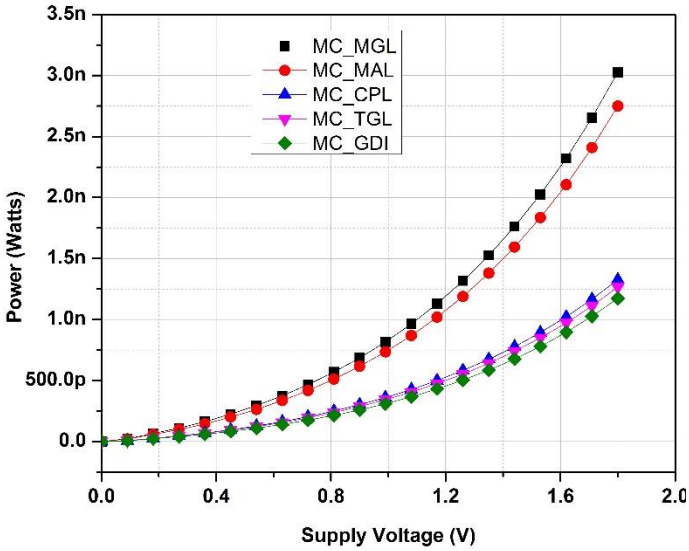

Figure 10 Variation of Power with Input Voltage of 4-bit MC

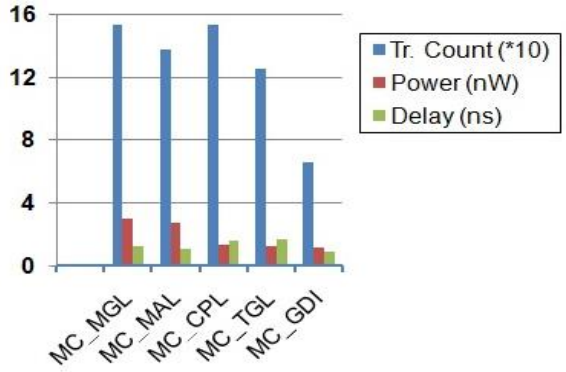

Figure 11 Performance Analysis of 4-Bit MC using various Logic Designs

Table 3 Performance Comparison of 4-bit MC using different digital logic styles.

Sr. No	Design Style	Number of Transistors	Power (nW)	Delay (ns)
1	MGL	154	3.027	1.269
2	MAL	138	2.750	1.062
3	CPL	154	1.327	1.608
4	TGL	126	1.267	1.688
5	GDI	62	1.173	0.932

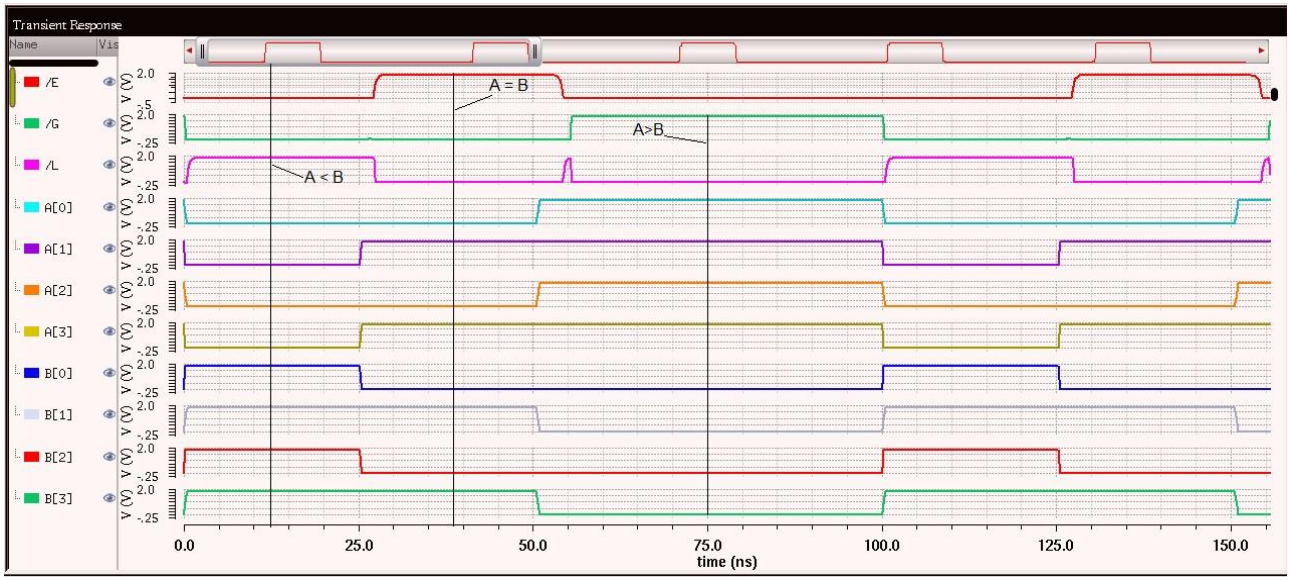

Figure 12 Simulation Results of 4-Bit Comparator using GDI logic obtained from Cadence spectre Environment

been designed and implemented using Majority Gate Logic (MGL), Mirror Adder Logic (MAL), Complementary Pass Transistor Logic (CPL), Transmission Gate Logic (TGL) and Gate Diffusion Input Logic (GDI). Simulations are accomplished in 180 nm CMOS process technology under the Cadence Spectre environment and are presented. From the simulation results, it is found that the GDI technique shows reduced power dissipation, increased speed, and a smaller area in terms of the transistor count compared to its counter logic design styles. Hence it is evident that the digital circuits implemented using the GDI technique exhibits superior performance and thus GDI technique proves to be the better option of a low-power design principle for VLSI circuit designer.

6. References

[1] Wang CC, Wu CF, Tsai KC. 1-GHz 64-bit high-speed comparator using ANT dynamic logic with two-phase clocking. IEE Proc Comput Digit Tech. 1998;145(6): 433-6.

[2] Kim JY, Yoo HJ. Bitwise competition logic for compact digital comparator. 2007 IEEE Asian Solid-State Circuits Conference; 2007 Nov 12-14; Jeju, South Korea. USA: IEEE; 2007. p. 59-62.

[3] Shekhawat V, Sharma T, Sharma KG. Low power magnitude comparator circuit design. Int J Comput Appl. 2014;94(1):22-4.

[4] Dubey V, Singh OP, Mishra GR. Design and implementation of a two-bit binary comparator using reversible logic. Int J Sci Res Publ. 2012;2(7):1-4.

[5] Agrakshi SR. Design and analysis of low power 2-Bit and 4-bit digital comparator in 45nm and 90nm CMOS technology. Int J Eng Tech Res. 2015;3(5):278-87.

[6] Deb S, Chaudhary S. High-speed comparator architectures for fast binary comparison. 2012 Third International Conference on Emerging Applications of Information Technology; 2012 Nov 30 – Dec 1; Kolkata, India. USA: IEEE; 2012. p. 454-7.

[7] Lam HM, Tsui CY. A MUX-based high-performance single-cycle CMOS comparator. IEEE Trans Circ Syst II. 2007;54(7):591-5.

[8] Weste N, Harris D. CMOS VLSI design: a circuits and system perspective. 3rd ed. USA: Addison-Wesley; 2004.

[9] Uyemura JP. Circuit design for CMOS VLSI. Norwell: Khuver Academic; 1992.

[10] Yano K, Tamanaka T, Nishida T, Saito M, Shimohigashi K, Shimizu A. A 3.8 ns CMOS 16 x 16-b Multiplier Using Complementary Pass-Transistor Logic. . IEEE J Solid State Circ. 1990;25(2):388-95.

[11] Avci M, Yildirim T. Complementary pass transistor logic synthesis with 123 decision diagram. J Electr Electron Eng. 2004;4(1):1045-9.

[12] Ghosh D, Nandy SK, Parthasarathy K, Visvanathan V. NPCPL: Normal process complementary pass transistor logic for low latency, high throughput designs. The Sixth International Conference on VLSI Design; 1993Jan 3-6; Bombay, India. USA: IEEE; 1993. p. 341-6.

[13] Shams AM, Darwish TK, Bayoumi MA. Performance analysis of low-power 1-bit CMOS full adder cells. IEEE Trans Very Large Scale Integr VLSI Syst. 2002;10(1): 20-9.

[14] Navi K, Maeen M, Foroutan V, Timarchi S, Kavehei O. A novel low-power Full Adder cell for low voltage. Integration. 2009;42(4):457-67.

[15] Wairya S, Nagaria RK, Tiwari S. Performance analysis of high speed hybrid CMOS full adder circuits for low voltage VLSI design. VLSI Des. 2012;2012:173079.

[16] Morgenshtein A, Fish A, Wagner IA. Gate-diffusion input (GDI) - a technique for low power design of digital circuits: analysis and characterization. 2002 IEEE International Symposium on Circuits and Systems; 2002 May 26-29; Phoenix-Scottsdale, AZ, USA. USA: IEEE; 2002. p. 477-80.

[17] Mukherjee DN, Panda S, Maji B. Performance evaluation of digital comparator using different logic styles. IETE J Res. 2018;64(3):422-9.

[18] Sucharitha, D. et al. GDI logic based design of hamming-code encoder and decoder for error free data communication. 2019 3rd International Conference on Computing Methodologies and Communication (ICCMC); 2019 Mar 27-29; Erode, India. USA: IEEE; 2019. p. 1-5.

[19] Bellaouar A, Elmasry MI. Low power digital VLSI design: circuits and systems. 2nd ed. Norwell: Kluwer academic; 1995.

[20] Rabaey JM. Digital integrated circuits. USA: Prentice-Hall; 1996.

[21] Rabaey JM, Chandrakasan A, Nikolic B. Digital integrated circuits, a design perspective. 2nd ed. New Jersey: Pearson educational publishers; 2008.

[22] Kandasamy N, Ahmad F, Reddy S, Ramesh Babu M, Telagam N, Utlapalli S. Performance evolution of 4-b bit MAC unit using hybrid GDI and transmission gate based adder and multiplier circuits in 180 and 90 nm technology. Microprocess Microsyst. 2018;59: 15-28.

[23] Kandasamy N, Mohan Kumar N, Telagam N, Ahmad F, Mishra G. Analysis of self checking and self resetting logic in CLA and CSA circuits using gate diffusion input technique. 2019 International Conference on Smart Systems and Inventive Technology (ICSSIT); 2019 Nov 27-29; Tirunelveli, India. USA: IEEE; 2019. p. 1-6.