

Design and analysis of modified recycling folded cascode amplifier with improved transconductance and slew rate

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Abstract

To improve the transconductance of operational transconductance amplifier (OTA), various architectures namely recycling folded cascode (RFC), Improved recycling folded cascode (IRFC), modified recycling folded cascode (MRFC) and high recycling folded cascode (HRFC) are existing in the literature. In this paper, further improvement in the transconductance of MRFC OTA can be achieved by shorting two nodes of its current mirror and is proposed as high modified recycling folded cascode (HMRFC) amplifier. The performance of the proposed HMRFC OTA is compared with the existing state of art OTAs. To validate the progressions in the specified parameters, recycling folded cascode (RFC), modified recycling folded cascode (MRFC) and high modified recycling folded cascode (HMRFC) OTAs are realized and implemented in UMC 180 nm process technology using Cadence Spectre for a bias current of 1.2 mA. Simulation results indicate that the proposed amplifier exhibits a DC gain of 79.47 dB, the slew rate of 194.2 V/ μ Sec, UGB of 285.85 MHz and phase-margin of 77.12° for a load capacitance of 5 pF and also observed that the CMRR and FoMs of the proposed amplifier are better by a factor of 1.3 and 1.5 in comparison to RFC, and by a factor of 1.27 and 1.41 in comparison to MRFC OTAs respectively.

Keywords: Transconductance, Modified recycling folded cascode, CMOS amplifiers, Unity gain bandwidth, Slew rate, Offset

1. Introduction

Most of the high-performance applications like analog to digital converters switched capacitive filters, wireless and mobile communications, bio-medical signal processors requires a high speed, low power and wide bandwidth portable electronic devices. This requirement made the researchers design such components with versatile performance metrics using existing CMOS technologies. Operational transconductance amplifier (OTA) is one such major block that plays a vital role in designing such systems.

Several OTA designs with various architectures are discussed in the state of art literature and have been selected based on the type of application. Folded cascode (FC) amplifier discussed in [1] is the most preferred architecture because of its high gain; high speed and larger output swing both for single and multistage amplifier design. Biasing NMOS transistors of conventional FC architecture is replaced by current mirrors in [2] to increase transconductance which improves the DC gain and slew rate. [3] Proposes a recycling OTA by introducing cross-coupled format in the differential pair output of conventional FC resulting in enhanced bandwidth, transconductance, and DC gain, but suffered from decay in phase margin. The problem

of the decaying phase margin of RFC OTA is addressed in [4] by including a phase margin network in the architecture. In [5] the performance of the RFC architecture has further increased by improving the transconductance by employing positive feedback. The improved recycling architecture of the folded cascode amplifier based on the separation of AC and DC currents paths for the enhancement of OTA parameters such as transconductance and unity-gain bandwidth is discussed in [6-7]. In [8], multipath recycling methods are used for enhancing the transconductance of a conventional FC amplifier. Current steering positive feedback based architecture for the performance improvement of RFC OTA in terms of DC gain is discussed in [9]. The DC gain and the transconductance of RFC is further improved by incorporating an extra current source in the architecture and termed as double recycling folded cascode amplifier is addressed in [10]. A novel technique of increasing output impedance for enhancing DC gain has been discussed in [11] and the architecture is termed as a modified recycling folded cascode amplifier (MRFC). [12], presented an FC OTA with improved DC gain, unity-gain bandwidth, and reduced power consumption by driving all the transistors in the sub-threshold region of operation. In [13], high recycling folded cascode (HRFC) architecture developed by

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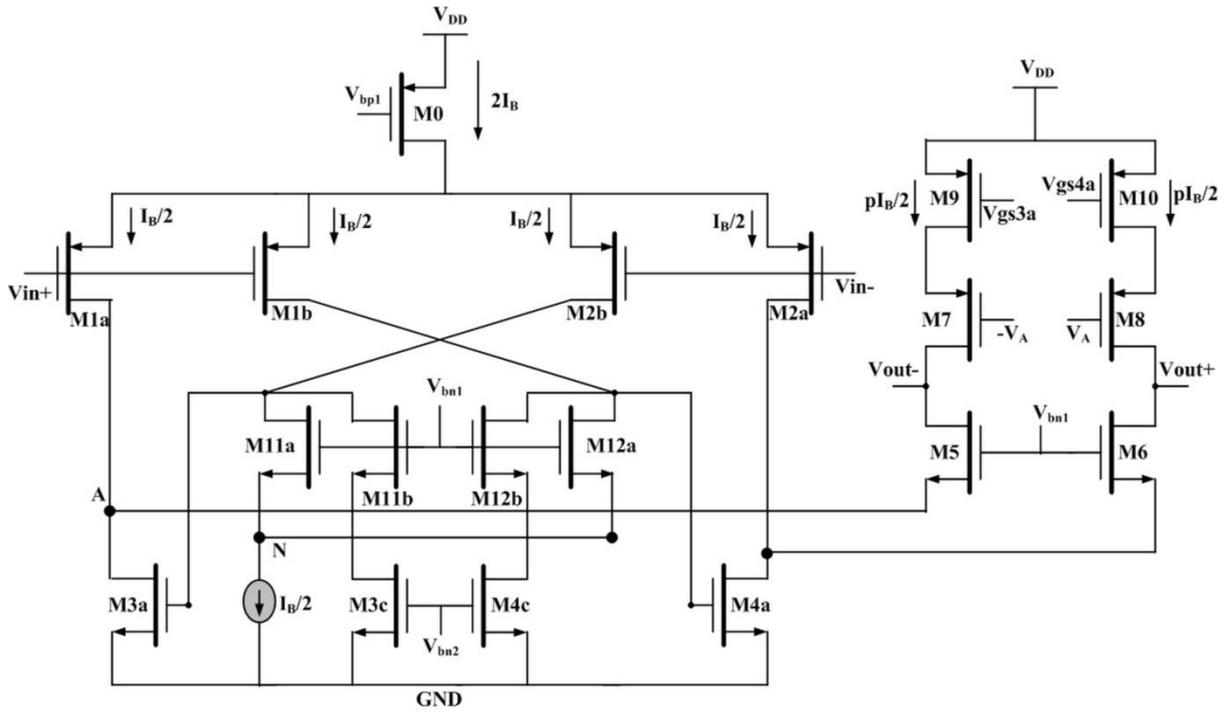


Figure 4 Illustrating the effect of Node N in HMRFC OTA.

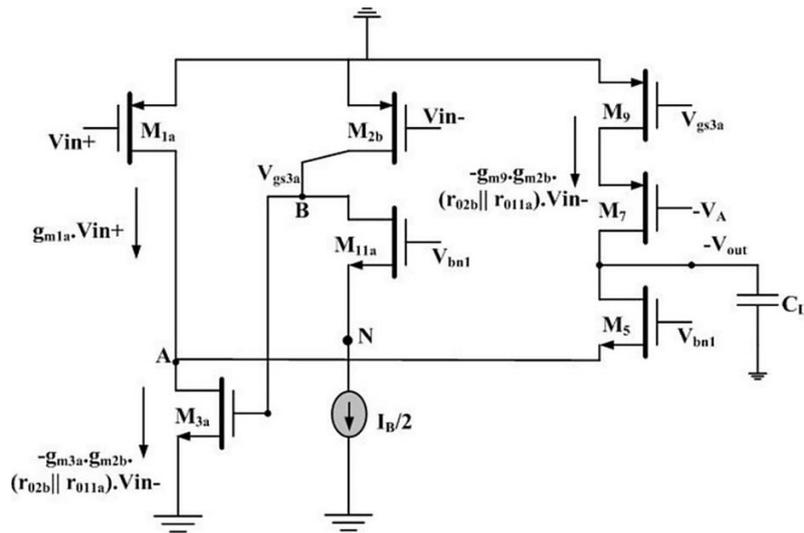


Figure 5 Half Circuit Transistor Model of Proposed HMRFC OTA.

to $gm1b \cdot (r_{01b} \parallel r_{012a})$ and $gm2b \cdot (r_{02b} \parallel r_{011a})$ when compared to 1 of MRFC [11].

The DC gain of the proposed OTA can be found by analyzing the circuit shown in Figure 4 for its effective small signal transconductance and output impedance.

3.1.1 Effective transconductance ($G_{M,HMRFC}$)

The effective small signal transconductance of the proposed HMRFC OTA can be obtained from the half circuit transistor model illustrated in Figure 5. The small-signal analysis can be done by considering the node voltages as shown in Figure 5 and shorting V_{out} to the ground and assuming is current flowing through the output node.

From Figure 5, it can be observed that the voltage at the drain of M_{2b} is expressed as,

$$V_{gs3a} = gm2b \cdot Vin- \cdot (r_{02b} \parallel r_{011a}) \tag{3}$$

The short circuit current after grounding the output V_{out} is expressed as,

$$I_s \cong Vin+ \cdot gm1a \cdot \left[1 + \frac{gm3a \cdot gm2b}{gm1a} \cdot (r_{02b} \parallel r_{011a}) + \frac{gm9 \cdot gm2b}{gm1a} \cdot (r_{02b} \parallel r_{011a}) \right] \tag{4}$$

Since the current flowing through M_{1a} and M_{2b} is the same, their transconductance remains to be the same i.e., $gm1a = gm2b$. The current flowing through the transistors M_{3a} and M_{1a} are in the ratio $(1+p):1$, hence their transconductance is also in the same ratio. Similarly, the transconductance ratio of the transistors M_9 and M_{1a} is $p:1$.

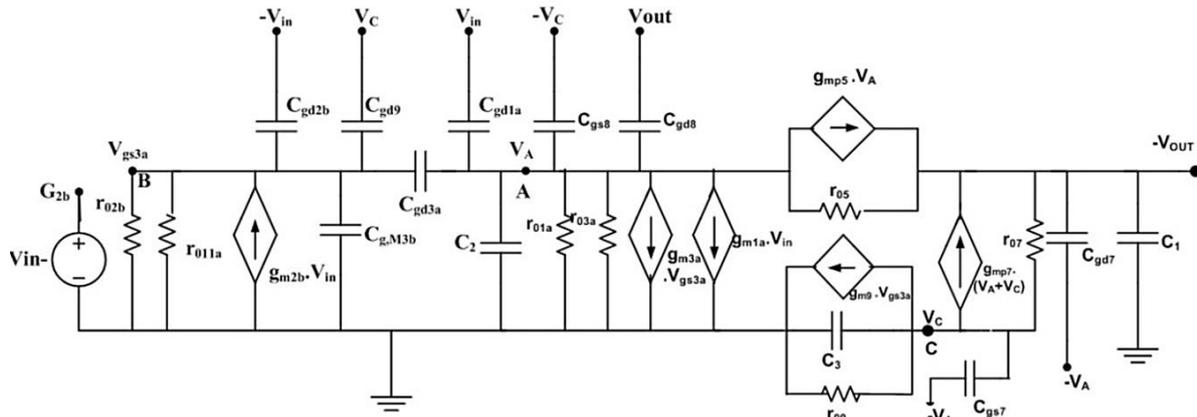


Figure 6 Half Circuit AC Equivalent Model of Proposed HMRFC OTA.

Substituting all the current and transconductance ratios in Eq. (4), the effective transconductance of the proposed HMRFC OTA is expressed as,

$$G_{m,HMRFC} = g_{m1a} \cdot [(1 + 2p) \cdot g_{m1a} \cdot (r_{02b} \parallel r_{011a}) + 1] \cong g_{m1a}^2 \cdot (1 + 2p) \cdot (r_{02b} \parallel r_{011a}) \quad (5)$$

Where, g_{m1a} is the small signal transconductance of input transistor M_{1a} . Eq. (5) depicts the enhancement in the small signal transconductance of proposed amplifier, in comparison to RFC and MRFC amplifiers.

3.1.2 Output impedance

The output impedance of the proposed amplifier is same as that of MRFC OTA and is expressed as,

$$R_{out,HMRFC} \cong r_{07} \cdot (g_{m7} + g_{mb7}) \cdot [r_{03a} \parallel (r_{03a} + r_{09})] \quad (6)$$

Where r_{oi} and g_{mi} is the output resistance and small signal transconductance of corresponding transistor i . Hence from Eq. (5) and Eq. (6), the DC-gain of the proposed OTA is expressed as,

$$A_V = G_{m,HMRFC} \cdot R_{out,HMRFC} = g_{m1a}^2 \cdot (1 + 2p) \cdot (r_{02b} \parallel r_{011a}) \cdot r_{07} \cdot (g_{m7} + g_{mb7}) \cdot [r_{03a} \parallel (r_{03a} + r_{09})] \quad (7)$$

Eq. (7) suggest that, in comparison to RFC and MRFC OTAs, the DC gain of the proposed amplifier is increased nearly by a factor of $g_{m1a} \cdot (r_{02b} \parallel r_{011a})$.

3.2 Frequency response

The frequency response of the proposed amplifier can be obtained from the high-frequency equivalent model derived from Figure 5 and shown in Figure 6. It can be observed from the equivalent model that the OTA exhibits 3 zeros and 4 poles the same as MRFC. Compared to MRFC, the dominant pole remains to be the same at the output, whereas non-dominant poles shifts to a node located at the gate terminal of M_{3b} or M_{4b} compared to node A of M_{3a} or M_{4a} . This shift in the non-dominant pole has resulted because of node N, which increases the resistance and capacitance at the gate terminal of M_{3b} or M_{4b} .

From Figure 6, the dominant pole frequency is expressed as,

$$\omega_{p1} \cong \frac{1}{R_{out,HMRFC} \cdot C_1} \quad (8)$$

Where $C_1 = C_L + C_{db5} + C_{gd5} + C_{db7}$ and $R_{out,HMRFC} \cong r_{07} \cdot (g_{m7} + g_{mb7}) \cdot [r_{03a} \parallel (r_{03a} + r_{09})]$.

The non-dominant pole frequency existing at the gate terminal of M_{3b} or M_{4b} can be expressed as,

$$\omega_{p2} \cong \frac{1}{R_{g,M3b} \cdot C_{g,M3b}} \quad (9)$$

Where $R_{g,M3b} = r_{011a} \parallel r_{02b}$ and $C_{g,M3b} = C_{db11a} + C_{ds2b} + C_{gb8} + C_{gs3b} + C_{gs3a}$

From Figure 6, it can be observed that the capacitor C_{gd3a} provides a feed forward path which results in a zero, whose frequency can be expressed as,

$$\omega_{z1} \cong \frac{g_{m3a}}{C_{gd3a}} \quad (10)$$

The unity gain bandwidth of the HMRFC OTA can be expressed as,

$$UGB_{HMRFC} = \frac{G_{m,HMRFC}}{C_1} \cong \frac{g_{m1a}^2 \cdot (1 + 2p) \cdot (r_{02b} \parallel r_{011a})}{C_1} \quad (11)$$

From Eq. (11), it can be observed that, the proper selection of p will results in increased UGB compared to RFC and MRFC amplifiers.

3.3 Slew rate

Slew rate at a node in the circuit is characterize as, the maximum rate of change of voltage for a change in unit time. Since the slew rate is directly related to the settling time of the circuit, it plays a vital role in the design of any amplifier circuit. The slew rate can be obtained by including a load capacitance (C_L) at the output and applying a large step signal at the inputs of the OTA. When the input V_{in+} in Figure 3 goes high, the transistors M_{1a} and M_{1b} are turned off that in turn shutoff the transistors M_{4a} , M_{4b} and M_6 which drives the transistor M_{2a} to cutoff and hence all the current $2I_B$ from tail source M_0 is insisted to flow through the transistor M_{2b} . This current is properly distributed as per the ratios among the paths of transistors M_{11a} - M_{3b} and M_{11b} - M_{3c} .

Table 1 Obtained transistor width (μm) for $L = 200 \text{ nm}$

DEVICE	RFC	MRFC	HMRFC
M0	110.4	110.4	110.4
M1a / M1b / M2a / M2b	22.4	22.4	22.4
M3a / M4a	19.28	19.28	19.28
M3b / M4b	7	3.5	3.5
M3c / M4c	-	11.33	11.33
M5 / M6	9.14	49	49
M7 / M8	108.5	108.5	108.5
M9 / M10	75	4.41	4.41
M11 / M12	7	-	-
M11a / M12a	-	3.5	3.5
M11b / M12b	-	15.93	15.93

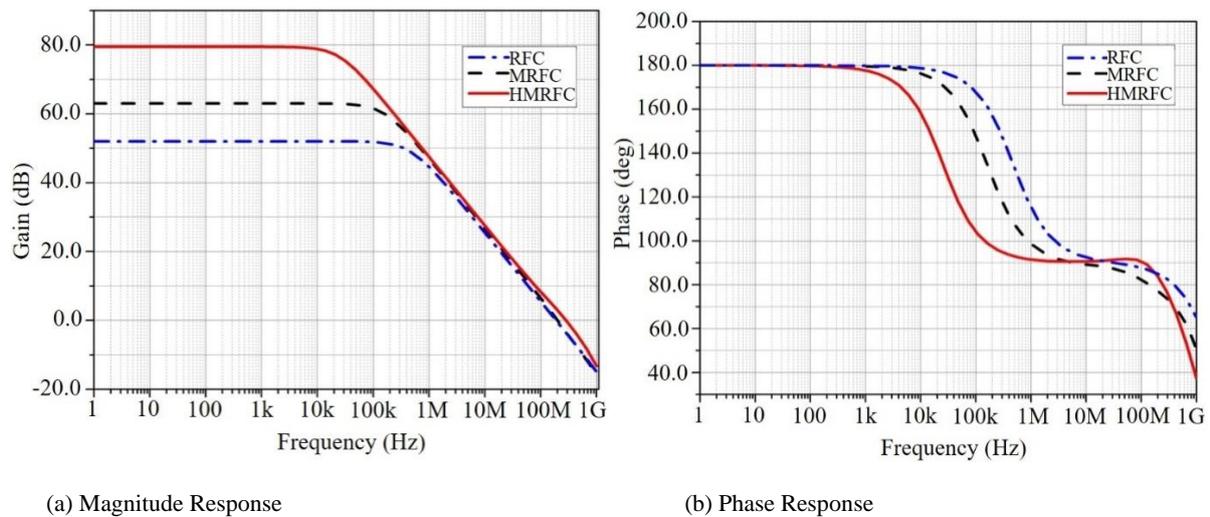


Figure 7 AC Frequency Responses of RFC, MRFC, and HMRFC OTAs

The current through the transistor M_{3b} is mirrored by $(1+p) : y$ and $p : y$ times into transistors M_{3a} and M_9 respectively. Hence M_9 source and M_{3a} sink current flows through the load capacitance C_L results in the slew rate. The slew rate of RFC, MRFC, and proposed HMRFC amplifier can be framed as,

$$SR_{RFC} = \frac{2kI_B}{C_L} \tag{12}$$

$$SR_{MRFC} = \frac{I_B(2-z)(1+x+u)}{y \cdot C_L} \tag{13}$$

$$SR_{HMRFC} = \frac{I_B(2-r)(1+2p)}{q \cdot C_L} \tag{14}$$

Eq. (14) guarantees that the proper selection of p , q and r leads to the improved slew rate of proposed OTA compared to RFC and MRFC amplifier configurations.

4. Simulation results

HMRFC with its counterparts RFC and MRFC are implemented in UMC 180 nm process technology with a bias current of $1200 \mu\text{A}$ at a supply-voltage of 1.8 V for a load capacitance of 5 pF . As shown in Figure 1, Figure 2 and Figure 3, the bias currents of all the three OTAs RFC, MRFC and HMRFC are considered in the ratios as, $k : 1$, $(1+x) : y : z$ and $(1+p) : q : r$ respectively. The transistors are simulated using the device sizes specified in Table 1. The

device sizes are selected based on the values of k , x , y , z , p , q , and r . For achieving better stability, the values of k , x , y , z , p , q , and r are selected as 3, 0.5, 0.25, 0.25, 2, 0.5 and 0.5 respectively. The simulation results of all three amplifiers are depicted in Figures 7 to 9. From the frequency response shown in Figure 7 of RFC, MRFC, and HMRFC OTAs, it is evident that the DC gain and unity-gain bandwidth of the proposed OTAs is found to be 79.47 dB and 285.85 MHz. The obtained DC gain is 27.47 dB and 16.4 dB more, while the UGB is 96 MHz and 83 MHz more than RFC and MRFC OTAs. The phase margin of RFC, MRFC and HMRFC OTAs are found to be 85.3° , 77.12° and 77.12° respectively. As shown in Figure 8, a large step voltage of 1.8 V_{PP} at 1 MHz is applied to study the slew rate performance of all the three OTAs. For the RFC, MRFC, and HMRFC, the average slew rates are obtained about $136.4 \text{ V}/\mu\text{sec}$, $171.3 \text{ V}/\mu\text{sec}$ and $194.2 \text{ V}/\mu\text{sec}$ respectively. The slew rate of the proposed amplifier is found to 1.4 and 1.1 times greater than its counterparts RFC and MRFC respectively. The CMRR of all the three configurations are 54.08 dB, 55.49 dB, and 70.76 dB respectively.

To study the performance metrics under power supply variations, the PSRR of all the three OTAs is obtained. The PSRR of RFC, MRFC, and HMRFC found to be 37.8 dB, 28.1 dB, and 41.6 dB respectively. To study the performance of proposed OTA under mismatch and process variations [15-17], the open-loop frequency response of the proposed amplifier is simulated using three process corners (TT, SS, and FF) and is depicted in Figure 9. The

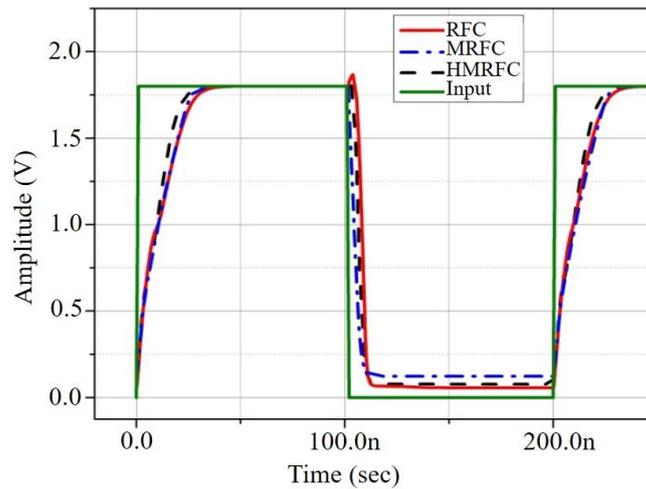


Figure 8 Step Responses of RFC, MRFC and HMRFC OTAs

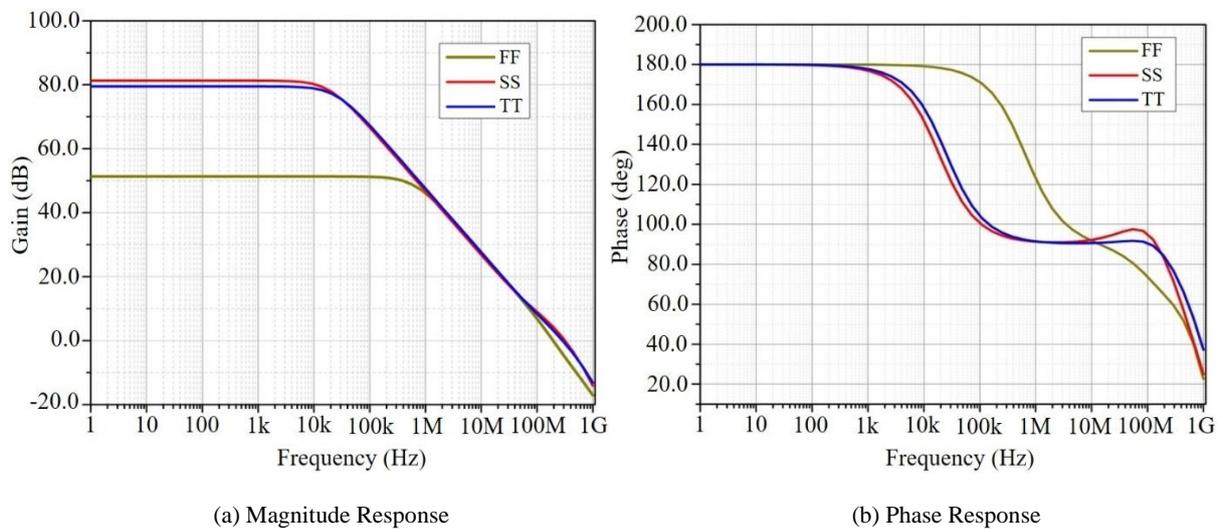


Figure 9 Frequency Response of Proposed OTA at different Process Corners

Table 2 Performance summary of RFC, MRFC and HMRFC OTAs

Parameter	RFC	MRFC	HMRFC
Supply Voltage (V)	1.8	1.8	1.8
Technology (nm)	180	180	180
Current (μA)	1200	1200	1200
Capacitive Load (pF)	5	5	5
DC Gain(dB)	52	63.1	79.47
Phase Margin (°)	85.31	77.77	77.12
Unity Gain Bandwidth (MHz)	189.25	202.43	285.85
Input Referred Noise @(1Hz-100MHz)(μ Vrms)	257.4	204.9	185.4
Slew rate(V/μsec)	136.4	171.3	194.2
Input offset voltage(3σ) (μ V)	22	4	7
CMRR (dB)	54.1	55.5	70.8
PSRR (dB)	37.8	28.1	41.6
FoM ₁ (MHz pF / mA)	788.5	843.4	1191
FoM ₂ ((V/μsec).pF/mA)	568.3	713.7	809.1
FoM ₃ (dB.MHz.(V/μsec).pF/V. (μ V/√Hz))	14.5k	29.7k	66.1k

performance summary of RFC, MRFC, and HMRFC amplifiers are tabulated in Table 2.

Table 3 shows the performance comparison of proposed OTA with some state of art literature with commonly measured Figure of Merits (FoMs) based on UGB slew rate,

noise and supply voltage. The expressions for FoM₁, FoM₂ and FoM₃ are,

$$FoM_1 = \frac{GBW \cdot C_L}{I_D} \tag{15}$$

Table 3 Performance Comparison of Proposed HMRFC OTA with RFC and MRFC OTAs

Parameter	[3] 2009	[6] 2012	[8] 2017	[9] 2014	[11] 2019	[13] 2018	[14] 2018	[18] 2015	[19] 2019	This Work
Supply Voltage (V)	1.8	1.2	1	1.2	1.8	0.6	1.5	1.8	1.8	1.8
Technology (nm)	180	130	180	90	180	180	180	180	180	180
Current (μ A)	800	300	50	560	300	1.25	37.5	400	1200	1200
Capacitive Load (pF)	5.6	5.5	15	5.6	5	20	1	4	5	5
DC Gain(dB)	60.9	64.9	66.9	62	76.24	58.9	53.4	63.4	73	79.47
Phase Margin ($^{\circ}$)	79.8	72.7	76.2	50	74.40	84.1	80.3	68.6	71	77.12
UGB (MHz)	134.2	67	6.4	164	74.7	0.066	20	89.0	247	285.85
Input Referred Noise @(1Hz-100MHz)(μ Vrms)	48.5	98.5	32.2	-	139.2	1.96 μ @ 1Hz	53.1	39.5	137	185.4
Slew rate(V/ μ sec)	94.1	20.7	1.86	39.3	64.05	0.0632	75	90.3	130	194.2
CMRR (dB)	-	-	-	-	-	-	86.8	-	84	70.8
PSRR (dB)	-	-	-	-	-	-	-	-	74	41.6
FoM ₁ (MHz pF / mA)	939.4	1229	1920	-	1245	1.1k	-	890	1029	1191
FoM ₂ (V/ μ sec).pF/mA)	658.7	379.5	558	393	1067	1.1k	-	903	541	809.1
FoM ₃ (dB.MHz.(V/ μ sec).pF/V. (μ V/ \sqrt Hz))	49.3k	4.18k	0.3k	-	7.28k	4.2	1k	29k	47k	66k

$$FoM_2 = \frac{SR \cdot C_L}{I_D} \quad (16)$$

$$FoM_3 = \frac{(DCgain) \cdot (UGB) \cdot (SR) \cdot C_L}{(SupplyVoltage) \cdot (Noise@1Hz - 100MHz)} \quad (17)$$

From Eq. (15) and (16), the figure of merit FoM₁ of proposed OTA is almost 1.5 times greater than RFC and 1.4 times greater than MRFC. Similarly, the calculations of FoM₂ in the proposed amplifier clarifies the enhancement in slew rate is around 1.43 times greater compared to RFC and 1.5 times greater compared to MRFC. Whereas FoM₃ illustrates the performance characteristics of proposed OTA is better compared to state of art literatures reported in Table 3.

5. Conclusion

In this paper, an improved version of the modified recycling folded cascode amplifier is discussed. Proposed OTA and existing OTAs are realized with the same power consumption and are compared. The proposed HMRFC amplifier illustrates better characteristics in terms of DC gain, transconductance, unity-gain bandwidth, slew rate, and noise in comparison to its counterparts RFC and MRFC OTAs. The enhancement in performance metrics is achieved because of the hybrid node created by the shorting of two nodes of MRFC. The proposed OTA has got higher FOM and is better suited for designing high speed analog to digital converters.

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