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Published by the Faculty of Engineering, Khon Kaen University, Thailand

A minimum power VCO design using an IMOS varactor for portable RF circuits

Vivek Jangra* and Manoj Kumar

University School of Information, Communication and Technology, Guru Gobind Singh Indraprastha University, New Delhi, India

Received 10 May 2019
Revised 14 July 2019
Accepted 15 July 2019

Abstract

This paper presents a wide tuning range voltage-controlled oscillator (VCO) circuit in 180 nm CMOS technology using an inversion mode MOSFET (IMOS) varactor in delay stages. Frequency variation in the VCO has been achieved by changing the capacitance of the output node with the use of an IMOS varactor comprised of two NMOS transistors connected in parallel. The VCO circuit uses a CMOS inverter and output frequency tuning that has been attained by varying the back-gate voltage (V_{sb}) and source/drain voltage (V_{ct}) of the IMOS varactor. Supply voltage variations from 1 V to 3 V achieves a tuning range from 0.280 GHz to 1.163 GHz along with power dissipation of 0.003 mW to 3.290 mW. Source/drain voltage (V_{ct}) variations from 0.1 V to 1.5 V achieve a tuning range of 0.685 GHz to 0.816 GHz along with power dissipation of 0.465 mW. Furthermore, the frequency varies from 0.810 GHz to 0.843 GHz with back-gate voltage (V_{sb}) tuning of the IMOS varactor. The results were obtained with different IMOS varactor widths and various combinations of supply voltages to achieve output frequency, power dissipation as well as phase noise. The VCO shows a phase noise of -102.81 dBc/Hz@1MHz and a figure of merit (FoM) is -162.10 dBc/Hz. The proposed VCO circuit attains reasonable performance results that are appropriate for low power radio frequency applications.

Keywords: Back-gate tuning, Delay cell, IMOS, Low power, Phase noise, Varactor

1. Introduction

Voltage-controlled oscillators (VCOs) are important circuit blocks in present and developing communication systems. VCOs with wide tuning ranges are used in modern radio frequency (RF) communication. These are an important constituent of the phase-locked loop (PLL) structure that is used for frequency synthesis and clock recovery [1-2]. VCO circuits with high frequencies find applications in waveform generators, frequency synthesizers, frequency demodulation, clock generators and sensor networks. Low power sensor networks have emerged as a significant research area for use in applications such as weather monitoring, space technology and defense surveillance. The prime considerations for VCO at design time are minimum area, low power consumption, high frequency and low phase noise [3]. In RF circuit design, VCOs consume the highest power. For this reason, low power consumption is a prerequisite for good performance [4]. To reduce the power consumption, a voltage scaling technique is widely used. The step-by step-downscaling of design technology presents many challenges to achieve low power and wider tuning ranges in VCO circuits. Various forms of VCO design implementations are reported in the literature such as LC-VCOs and CMOS VCOs [5-8]. A LC VCO shows a higher operational frequency and good phase noise performance due to the large quality factor attainable with resonant networks. However, the use of inductors in a CMOS design requires a large chip layout area and provides a limited tuning range. CMOS-based ring VCOs are preferred due to their simple design optimization, large tuning range and small chip area [9]. A ring VCO is composed of an odd number of single-ended or even/odd number of differential delay stages. Also, pseudo-differential topologies have been reported and are preferred due to high voltage swings, moderate phase noise performance and low power consumption [10]. Forward body biasing techniques reduce the threshold voltage with a lower supply voltage. However, it increases the leakage current and results in higher power consumption [11]. With recent scaling trends of CMOS technology, reduction in leakage current is considered an important issue. Therefore, multi-threshold voltage techniques have been used to reduce leakage current [12]. Cross coupled transistor configurations feature low power consumption but fail to achieve a wider tuning range [13]. The transformer coupled varactor configuration helps to achieve wide tuning range [14]. To maintain wide frequency tuning and higher Q factor in VCOs, low-loss varactors are desirable [15]. A varactor-coupled quadrature VCO increases the linear tuning range by biasing varactors at various voltages [16]. A varactor is generally used to obtain variable capacitance. Increased silicon doping

*Corresponding author.
Email address: pec.vivek@gmail.com
doi: 10.14456/easr.2019.37

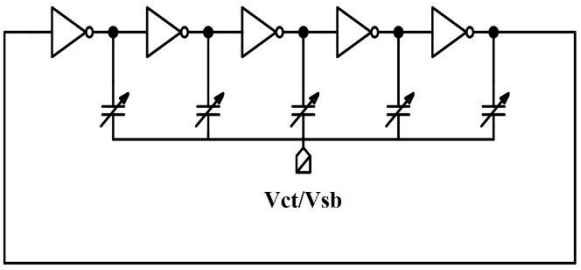


Figure 1 Proposed architecture of a ring VCO.

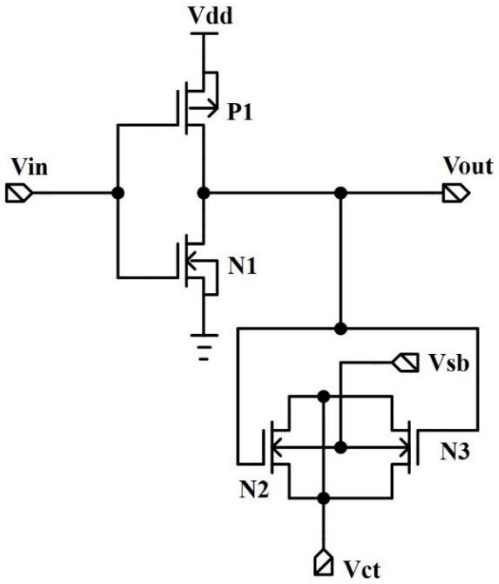


Figure 2 Proposed delay cell.

decreases phase noise and resistive losses, thereby increasing the Q-factor of MOSFET varactors [17-19]. An IMOS varactor is like a MOS transistor with a gate as the first terminal and the drain (D), bulk (B) and source (S) linked to form the other terminal. The change in the bulk to gate node voltage (V_{bg}) regulates the variation rate of MOS capacitance. MOSFET varactors work in three regions: accumulation, inversion and depletion. The inversion and accumulation regions have a maximum capacitance per unit area [20]. All three operating modes depends on the value of the threshold voltage ($|V_{th}|$) and bulk to gate node voltage (V_{bg}). In the accumulation region, $V_{bg} < V_{fb}$ where V_{fb} is the flat band voltage. In this region, the threshold voltage is greater than the bulk voltage. For the depletion region $V_{fb} < V_{bg} < |V_{th}|$, i.e., voltage between bulk and gate is smaller than the threshold voltage and higher than the flat band voltage. In the inversion region, $V_{bg} > |V_{th}|$, i.e., the threshold voltage must be less than the bulk and gate voltages with a higher carrier concentration beneath the gate oxide resulting in freely moving charge carriers [21]. For MOS transistors, the tuning of the bulk terminal decreases the power dissipation and reverse body biasing minimizes the delay in the circuit [22]. IMOS offers lower power dissipation and good phase noise performance [23].

In the literature, various methods of VCO tuning have been reported [24-27]. These include complementary current control, dual delay path, stabilized current level, multiple feedback loops, varactor tuning and output load variations. In the reported VCO, two NMOS were used in parallel to achieve an inversion mode (IMOS) varactor. The delay stage tuned by an IMOS varactor offers lower power dissipation, a higher frequency range and lower phase noise. The rest of the paper is arranged as follows. Section 2 explains the VCO circuit description and IMOS modelling. Section 3 presents the results and discussion. Section 4 offers conclusions based on this work.

2. VCO circuit design and IMOS modelling

A ring VCO is a special oscillator that is comprised of delay stages. Each stage provides input to the next stage in the ring. In a CMOS ring VCO, the output of last stage is given as feedback to the input of first stage. In a single ended topology, the number of delay stages must be odd. For a ring VCO, if N is the number of inverters in the chain and τ_d is the time delay for a single stage, the frequency of oscillation is given by Equation (1).

$$f_o = \frac{1}{2N\tau_d} \tag{1}$$

The number of stages must be decreased to increase the oscillation frequency. Figure 1 depicts the architecture of the proposed ring VCO. Figure 2 shows the delay stage of the proposed ring VCO, which consists of a basic CMOS inverter with an IMOS varactor for frequency tuning in delay stages. Frequency tuning is accomplished by varying the power supply voltage (V_{dd}) of the ring VCO, back-gate voltage (V_{sb}) and source/drain voltage (V_{ct}) of the IMOS varactor.

The MOS transistor sizing for the proposed delay cell with a gate length of 0.18 μm is given in Table 1.

Table 1 MOS Transistor sizing for the VCO.

Transistors	Width/Length
P1	2/0.18
N1	0.5/0.18
N2, N3	5/0.18

An important scaling factor to maintain MOSFET efficiency is the threshold voltage (V_{th} *or* V_t). It is the minimum gate-to-source voltage (V_{gs}) that is required to form a conducting path amongst the source and the drain terminals. The threshold voltage for a non-zero substrate bias voltage ($V_{sb} > 0$) is expressed by Equation (2).

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\phi_f + V_{sb}}\right) - \sqrt{2\phi_f} \tag{2}$$

where V_{th0} is the threshold voltage for $V_{sb} = 0$, ϕ_f is the substrate Fermi potential, and γ is a fabrication-process parameter, known as the body-effect parameter. For a MOS transistor in inversion mode, the threshold is given by Equation (3).

$$V_{th} = V_{fb} - \frac{\sqrt{2\varepsilon_{si}qN_A(2|\phi_f| + |V_C - V_B|)}}{C_{ox}} - 2|\phi_f| + V_C - \frac{Q_i}{C_{ox}} \tag{3}$$

where V_{fb} denotes the flat band voltage, Q_i denotes the ionized donors charge, q symbolizes the electronic charge, N_A is the p-type dopant concentration, C_{ox} denotes the gate oxide capacitance, ε_{si} represents the dielectric constant of

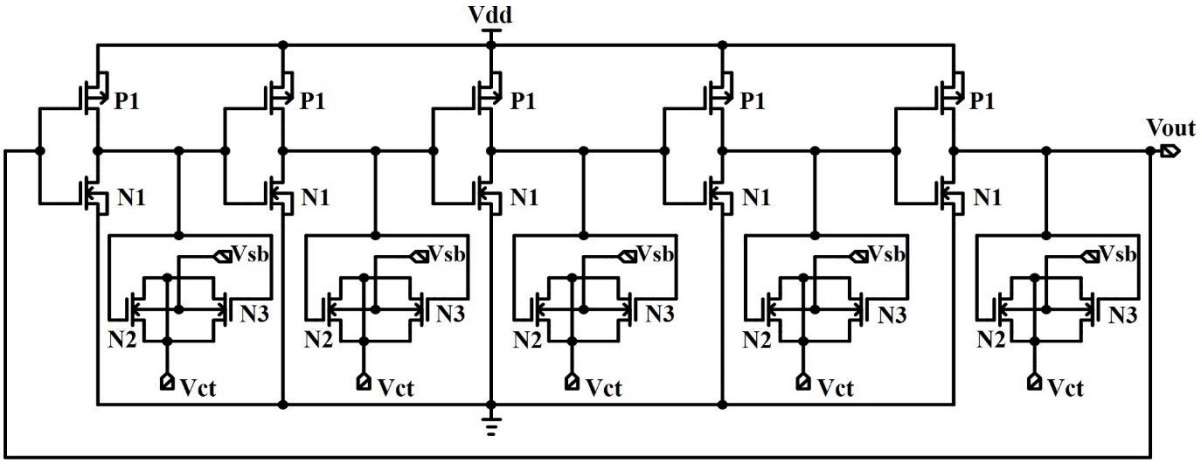


Figure 3 Five stage ring VCO structure.

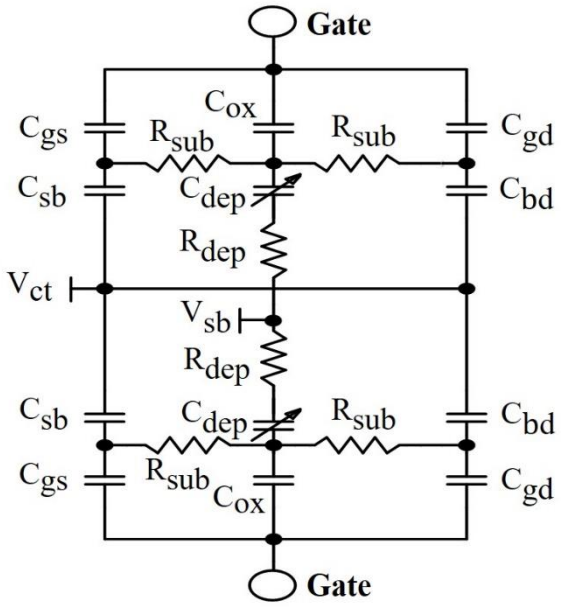


Figure 4 Simplified equivalent model of IMOS varactor capacitance

silicon and ϕ_f represents substrate Fermi potential. For an IMOS varactor made from NMOS transistors, mobile electrons create an inversion channel where $V_{gs} > |V_{th}|$, which is the condition of inversion for an IMOS varactor. The oxide capacitance in this region is presented by Equation (4).

$$C_{ox} = \frac{\varepsilon . W . L}{t_{ox}} \tag{4}$$

where $W.L$ denotes the transistor channel area, ε is the dielectric constant and t_{ox} is the thickness of oxide. This area relies on the channel width of the IMOS transistor.

A five-stage ring VCO is designed with the proposed delay stage and presented in Figure 3. The output of primary stage is linked to the input of second stage and continues to the last stages. Output of the last stage is linked to the first stage in the form of a closed feedback loop. The IMOS varactor in the proposed ring VCO changes the load capacitance, which enhances the single ended delay. IMOS varactors have two nodes. The back-gate voltage (V_{sb}) is connected to the body terminal and the source/drain voltage (V_{ct}) node controls the capacitance of the varactor through a control voltage. Initially, the back-gate voltage port is grounded. As the source/drain voltage increases in an IMOS circuit, a greater number of electrons come into the channel decreasing the capacitance. Back-gate biasing of NMOS affects the threshold voltage, which impacts substrate resistance/capacitance, and therefore, the maximum frequency tuning is achieved. A simplified equivalent model for IMOS varactor capacitance is presented in Figure 4 [11].

Here, C_{dep} is the capacitance of the channel, C_{ox}. It represents the oxide capacitance between the substrate and the gate. C_{gs} represents the parasitic capacitance from gate to source and C_{gd} is the parasitic capacitance from gate to drain. C_{sb} is the source to bulk capacitance and C_{bd} is the bulk to drain capacitance, R_{sub} is the substrate resistance and R_{dep} is the depletion resistance. In a MOS varactor, the capacitance between the substrate and the gate is a series connection of depletion region capacitance C_{dep} and gate oxide capacitance C_{ox}. It is given by Equation (5).

$$C_{eq} = \frac{1}{\left(\frac{1}{C_{ox}} + \frac{1}{C_{dep}}\right)} \tag{5}$$

With increased source/drain voltage, the depletion region width increases at the source end which decreases the bulk to source capacitance, leading to a decrease in capacitance between the gate terminals. The decreased capacitance also decreases the time delay of each cell which gives rise to the output frequency of the VCO. With the increase in negative back-gate voltage, many holes are drawn from the substrate terminal and decrease the depletion width. This decrease in depletion width reduces the depletion capacitance which also reduces the propagation delay resulting in an increase in the output frequency. In the other case, both back-gate voltage and source/drain voltage are applied to obtain the frequency variations as depicted in Figure 3.

3. Results and discussions

The proposed five-stage ring VCO has been designed in TSMC 180 nm CMOS technology and the results were obtained with SPICE simulations in Mentor Graphics EDA tool. Various VCO analyses have been performed to achieve power dissipation, frequency range and phase noise with

Table 2 Effect of source/drain voltage (V_{ct}) variations on output frequency at V_{dd} = 1.8 V and V_{sb} = 0 V with different IMOS widths.

V_{ct}	Frequency (GHz)				Power Dissipation (mW)
(V)	W_I = 5µm	W_I = 10µm	W_I = 15µm	W_I = 20µm	
0.1	0.685	0.363	0.251	0.192	0.465
0.3	0.694	0.386	0.267	0.204	
0.5	0.729	0.408	0.282	0.216	
0.7	0.767	0.431	0.299	0.229	
0.9	0.799	0.450	0.314	0.240	
1.1	0.814	0.460	0.321	0.247	
1.3	0.815	0.461	0.322	0.248	
1.5	0.816	0.462	0.323	0.249	

Table 3 Effect of power supply voltage (V_{dd}) variations on output frequency at V_{ct} = 1 V and V_{sb} = 0 V with different IMOS widths.

V_{dd}	Frequency (GHz)				Power Dissipation (mW)
(V)	W_I = 5µm	W_I = 10µm	W_I = 15µm	W_I = 20µm	
1.0	0.280	0.158	0.110	0.084	0.003
1.2	0.431	0.243	0.169	0.130	0.027
1.4	0.572	0.323	0.225	0.173	0.106
1.6	0.699	0.395	0.276	0.212	0.252
1.8	0.810	0.457	0.319	0.245	0.465
2.0	0.885	0.500	0.349	0.267	0.748
2.2	0.947	0.533	0.371	0.284	1.103
2.4	1.001	0.562	0.391	0.299	1.532
2.6	1.042	0.585	0.406	0.311	2.039
2.8	1.079	0.603	0.418	0.321	2.625
3.0	1.163	0.618	0.428	0.328	3.290

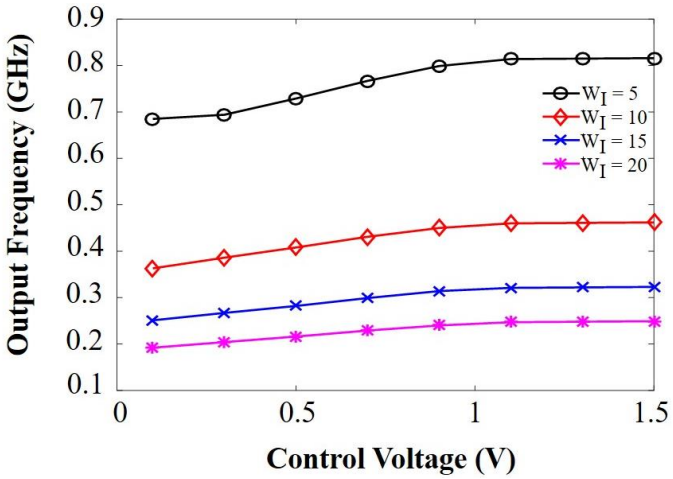


Figure 5 Effect of source/drain voltage (V_{ct}) variation on the output frequency with different IMOS widths (W_I)

changes in the IMOS varactor widths such as 5, 10, 15 and 20 µm. The results of proposed five-stage ring VCO with changes in IMOS source/drain voltage (V_{ct}) from 0.1 V to 1.5 V are shown in Table 2. As V_{ct} increases, the IMOS capacitance decreases, which increases the output frequency of the VCO. The results were generate for various IMOS widths (W_I). The capacitance of an IMOS increases with increased IMOS width (W_I) and as a result, the output frequency decreases as shown in Table 2. The power dissipation of the VCO is 0.465 mW. For various IMOS widths (W_I), the effect of source/drain voltage (V_{ct}) variations on the output frequency is presented in Figure 5. Table 3 presents the changes in output frequency for power supply voltage (V_{dd}) variations from 1 V to 3 V along with power dissipation for various IMOS varactor widths (W_I). Due to the increase in the power supply voltage (V_{dd}), the biasing current increases in the delay cell, resulting in a higher output oscillation frequency. Changes in the supply voltage from 1 V to 3 V reflects power dissipation from 0.003 mW to 3.290 mW for the proposed ring VCO. Figure 6 depicts the effect of power supply voltage (V_{dd}) variations for dissimilar IMOS widths (W_I).

Figure 7 presents the variations in power dissipated by the VCO against power supply voltage variations. Table 4 presents the effect of back-gate voltage (V_{sb}) variations from 0 V to -1.0 V on the output frequency of the proposed VCO with various IMOS widths (W_I). Moreover, the proposed VCO dissipates 0.465 mW of power for varying back-gate voltage. With the increases in the back-gate voltage, the biasing current in the delay cell increases, which

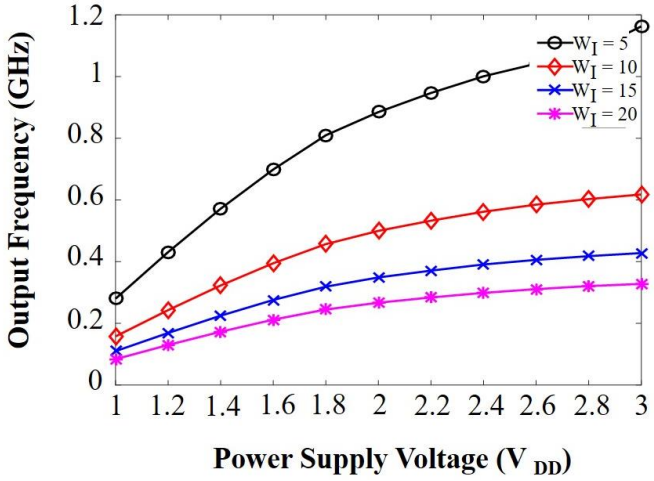


Figure 6 Change in output frequency for power supply voltage variations with different IMOS widths (W_I)

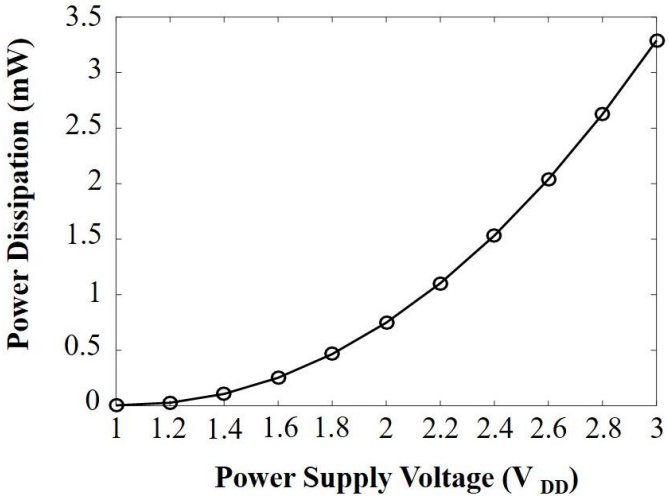


Figure 7 Change in dissipated power against power supply voltage variations.

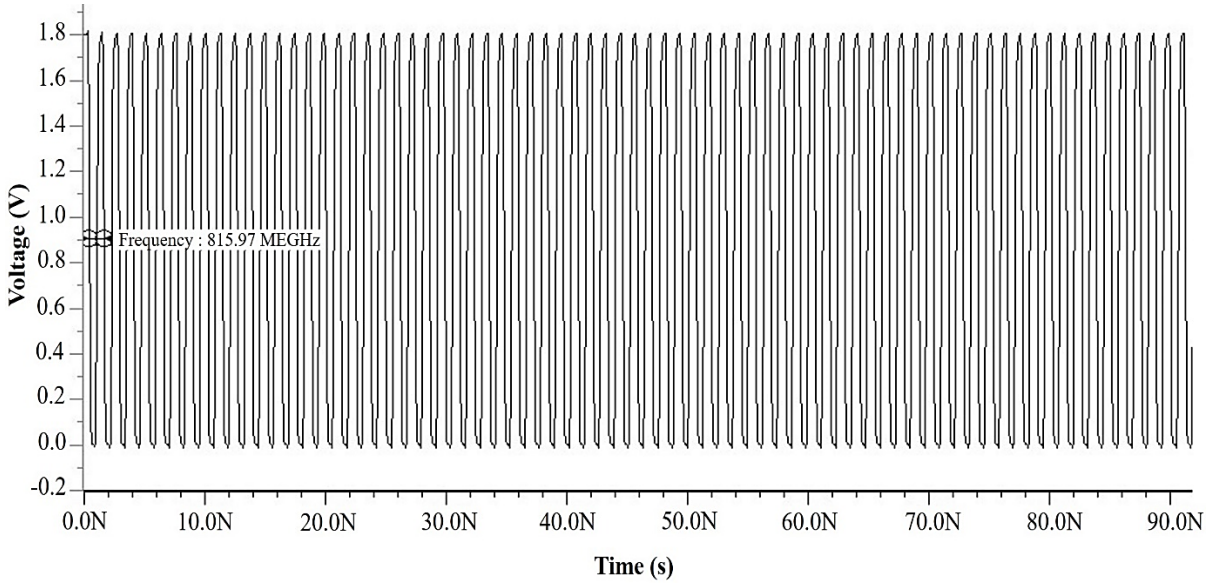
Table 4 Effect of back-gate voltage (V_{sb}) variations on the output frequency at V_{dd} = 1.8 V, V_{ct} = 1 V with different IMOS widths.

V_{sb} (V)	Frequency (GHz)				Power Dissipation (mW)
	W_I = 5 µm	W_I = 10 µm	W_I = 15 µm	W_I = 20 µm	
0	0.810	0.456	0.319	0.245	0.465
-0.1	0.816	0.462	0.322	0.247	
-0.2	0.820	0.464	0.324	0.249	
-0.3	0.823	0.466	0.326	0.250	
-0.4	0.826	0.468	0.327	0.251	
-0.5	0.829	0.470	0.328	0.252	
-0.6	0.831	0.471	0.329	0.252	
-0.7	0.833	0.472	0.330	0.253	
-0.8	0.835	0.473	0.331	0.254	
-0.9	0.838	0.474	0.332	0.255	
-1.0	0.843	0.475	0.333	0.256	

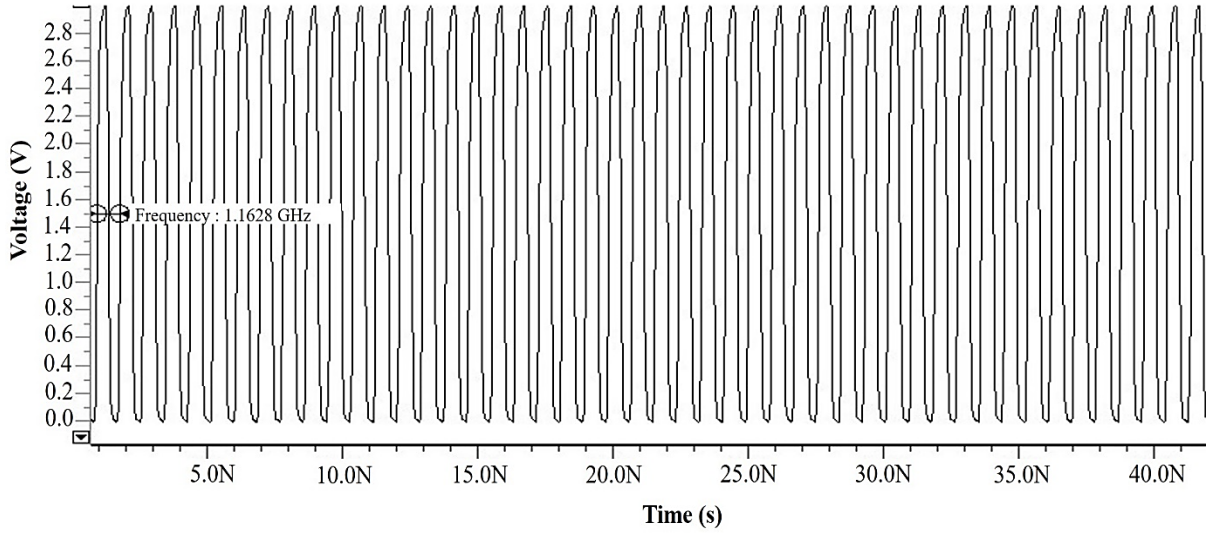
reduces the propagation delay resulting in a higher frequency at the output. The VCO output frequency waveforms at dissimilar voltage tuning conditions are presented in Figure 8 (a), (b) & (c).

Phase noise is a key parameter as it governs the overall performance of a ring VCO. Table 5 shows the outcomes of the phase noise performance at different groupings of VCO tuning voltages with an offset of 1 MHz from the carrier. The reported VCO depicts a phase noise of −102.81 dBc/Hz@1 MHz. The phase noise plots are shown in Figure 9 (a), (b) & (c) for various groupings of VCO tuning voltages. The figure-of-merit shows the VCO performance and is given by Equation (6) [28].

$$FOM = L\{\Delta f\} - 20\,log\left(\frac{f_o}{\Delta f}\right) + 10\,log\left(\frac{P_{DC}}{1\text{mW}}\right) \quad (6)$$



(a)



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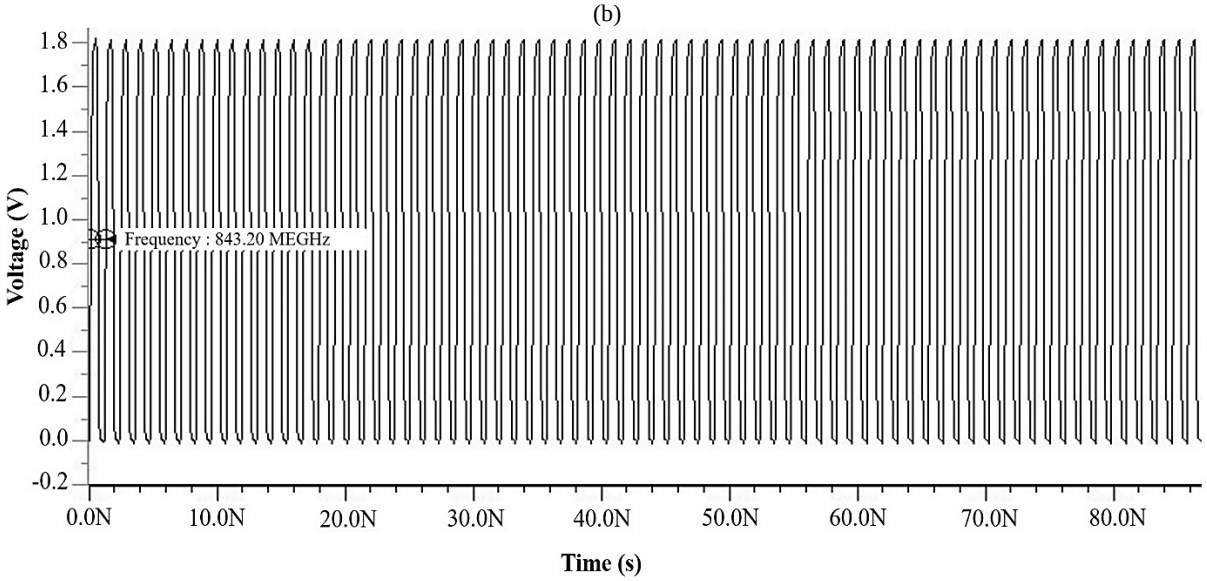

(c)

Figure 8 Output frequency waveforms for (a) power supply voltage tuning at V_{dd} = 1.8 V, V_{ct} = 1 V and V_{sb} = 0 V, (b) source/drain voltage tuning at V_{dd} = 1.8 V, V_{sb} = 0 V and (c) back-gate voltage tuning at V_{dd} = 1.8V, V_{ct} = 1V

Table 5 Outcomes of the phase noise measurements for the proposed ring VCO

Power Supply Voltage (V_{dd})	Control Voltage ($V_{control}$) of IMOS	Back-gate Voltage (V_{sb}) of IMOS	Width of IMOS (W_l) (µm)	Phase noise (dBc/Hz)	Output Frequency (GHz)	Power Dissipation (mW)	Figure of Merit (FoM)
2.4V	0V	-1.0V	5	-106.31	1.358	1.53	165.3
1.8V	1.0V	0V	5	-102.94	0.810	0.465	162.3
1.8V	1.0V	-0.5V	5	-102.81	0.828	0.465	162.1
1.8V	1.5V	-1.5V	5	-102.26	0.841	0.465	162.7
1.8V	0.5V	-1.0V	5	-101.28	0.776	0.465	160.3
1.0V	1.0V	-1.0V	5	-100.62	0.290	0.003	167.3

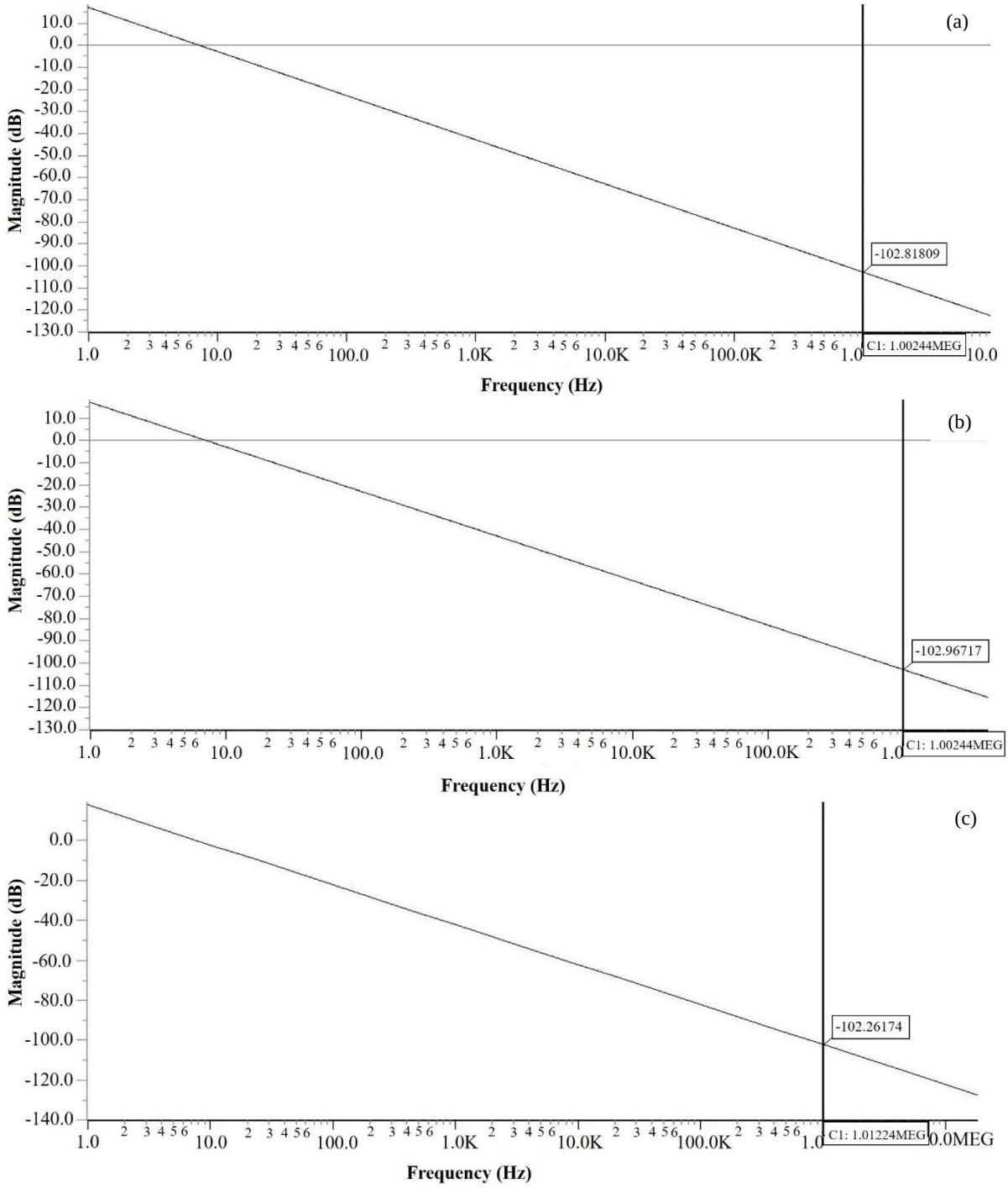

Figure 9 Phase noise results at (a) V_{dd} = 1.8 V, V_{ct} = 1.0 V & V_{sb} = 0 V (b) V_{dd} = 1.8 V, V_{ct} = 1.0 V & V_{sb} = -0.5 V & (c) V_{dd} = 1.8 V, V_{ct} = 1.5 V & V_{sb} = -1.5 V

Table 6 Summary of the performance of the proposed VCO compared with prior studies.

References	Frequency Range (GHz)	Technology (μm)	Phase Noise (dBc/Hz)	Power Dissipation (mW)	FoM (dBc/Hz)
[3]	1.7-2.3	0.18	-98.2@1MHz	6	-
[4]	0.02-0.80	0.18	-108@1MHz	22	150.6
[7]	1.75-1.93	0.18	-102@1MHz	13	156.3
[15]	5.19-5.93	0.18	-99.5@1MHz	80	155.72
[19]	0.51-1.28	0.18	-90@1MHz	0.71	151.48
[26]	4.21-5.92	0.18	-99.1@1MHz	58	156.28
[27]	7.33-7.86	0.13	-103@1MHz	60	163.3
Current Study	0.280 to 1.1628 (Power supply tuning) 0.685–0.816 (IMOS source/drain tuning) 0.810 to 0.843 (IMOS back-gate tuning)	0.18	-102.8@1MHz	0.465	162.1

In the above equation, $L\{\Delta f\}$ is the phase noise in dBc/Hz at offset frequency Δf from the carrier frequency f_o, Δf is the frequency offset, f_o is the carrier frequency, P_{DC} is the power dissipated in mW. The FoM for the proposed VCO varies from 160.3 dBc/Hz to 167.3 dBc/Hz for dissimilar tuning voltages.

Comparison results of the proposed ring VCO with earlier reported VCOs [3, 4, 7, 14, 19, 21, 22] in power dissipation, frequency tuning, phase noise and figure of merit are shown in Table 6. The reported VCO dissipates less power with a wider frequency range and good phase noise with an acceptable FoM.

4. Conclusions

In this paper, a new VCO design is presented with five delay stages. Each delay stage has one CMOS inverter and an IMOS varactor. Output frequency tuning is achieved with variations in power supply voltage (V_{dd}), back-gate voltage (V_{sb}) and source/drain voltage (V_{ct}) of the IMOS varactor. Source/drain voltage tuning of IMOS varactor with various widths gives a tuning range of 17.4%, 24%, 25% and 25.85% for the proposed VCO. Likewise, output frequency variation in power supply voltage tuning and back gate voltage tuning has been attained. For the proposed VCO, power dissipation of 0.465 mW, 0.00 3mW to 3.290 mW and 0.465 mW was attained with source/drain voltage tuning, power supply voltage tuning and back-gate voltage tuning, respectively. Moreover, the VCO attains a phase noise of −102.81 dBc/Hz@1 MHz. The figure of merit (FoM) varies from -160.3 dBc/Hz to -167.3 dBc/Hz for dissimilar voltage tunings. The reported VCO architecture has better results in terms of a wide tuning range, better phase noise performance at low power consumption with an acceptable figure of merit. The proposed VCO offers substantial improvements in applications of modern low power radio frequency circuits.

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