วิศวกรรมสาร มข. ปีที่ 37 ฉบับที่ 3 (201-208) กรกฎาคม –กันยายน 2553 บทความวิชาการ
KKU Engineering Journal Vol.37 No.3 (201-208) July – September 2010

On-Chip Active Inductors: The Promising Replacements of the On-Chip Passive Inductors

Rawid Banchuin*

Abstract

On-chip inductors have been found to be applicable in many applications for example, filter, power convertor and oscillator. The on-chip active inductors have many advantages over their passive counterparts for example, independency of inductance value from chip area, electronically tuning capability, higher Q-factor, applicability at kHz-MHz range and cost effectiveness. So, they have been found to be the promising replacement of the on-chip passive inductors. Hence, this paper focuses on the overview of the on-chip active inductors. The fundamental concept and examples of on-chip active inductors are addressed. The performance comparison of the on-chip active inductors is also discussed. This paper should be very useful to those who interest in the design and development tasks involving on-chip active inductors.

Keywords: On-chip inductors, On-chip active inductor, Network level based on-chip active inductor, Transistor level based on-chip active inductor, On-chip passive inductor

*Lecturer, Department of Computer Engineering, Siam University, Bangkok 10160,
E-mail: rawid_b@yahoo.com

1. Introduction

On-chip inductors have been found to be applicable in many analog/mixed signal circuits and systems for example, filter, power convertor and oscillator. They can be realized both as passive elements and active circuits which entitled on-chip passive inductor and on-chip active inductor respectively.

On-chip active inductors have many advantages over the passive ones for example, independency of inductance values from chip areas, electronically tuning capability, higher Q-factors, applicability at kHz-MHz range and cost effectiveness. So, they have been found to be the promising replacements. Many articles which focus on the overview of the on-chip passive inductors have been proposed for example, (Chen, Liou, 2004). So, the similar article which focuses on the on-chip active inductor has been found to be interresting.

Hence, this paper focuses on the overview of the on-chip active inductors. The fundamental concept of the on-chip active inductors will be firstly addressed followed by some examples of the proposed on-chip active inductors. The discussion on the performance comparison of the on-chip active inductors will be given afterward. This paper should be useful to those who interest in the design and development of any applications involving on-chip active inductors.

2. Fundamental Concept

On-chip active inductors are actually the active networks with the inductive impedance functions. Traditionally, it can be constructed by loading the gyrator with the capacitance. Generally, the gyrator is a two port network with the following admittance matrix (Green, 1996)

$$Y = \begin{bmatrix} 0 & -g_1 \\ g_2 & 0 \end{bmatrix}. \quad (1)$$

The symbol of the gyrator can be depicted as follows (Singer, 1988)

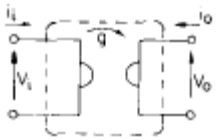

Figure 1 *Symbol of the gyrator (Singer, 1988)*

The gyrator can be constructed by using various active elements. So, the active network which simulates the inductor can be obtained by loading the gyrator with the capacitance. This active network is entitled the active inductor or the on-chip active inductor at the IC level.

Let the value of the load capacitance be C, the effective inductance (L) of the resulting on-chip active inductor can be given by (Green, 1996)

$$L = \frac{C}{g_1 g_2} \quad (2)$$

According to (Banchuin et.al, 2008), the on-chip active inductors can be divided into two categories. The first category composes of those constructed at the network level basis by using the available on-chip active building blocks for example, OP-AMP, OTA, CDBA and Current Conveyor of various generations for constructing the gyrator along with the on-chip nominal capacitor for being the load capacitance. These on-chip active inductors are categorized as the network level based on-chip active inductors.

On the other hand, those of the second category are constructed at the transistor level basis by using only small number of transistors for the gyrator realization. They use on the parasitic capacitances of the basis transistors in order to realize the load capacitance without any nominal capacitor required. These on-chip active inductors

can be categorized as the transistor level based on-chip active inductors.

In the subsequent sections, some examples of the on-chip active inductors of both categories will be mentioned.

3. Network Level Based On-Chip Active Inductors

Some examples of the on-chip active inductor of this category will be discussed in this section.

3.1 OTA-based inductor

Traditionally, the OTA-based inductor can be constructed by the realization of the gyrator with the OTAs and let the nominal capacitor be the load as proposed in (Geiger, Sanchez-Sinencio, 1985) which can be depicted as follows

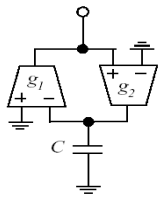

Figure 2 *The OTA-based inductor*

For OTA-based inductor, $g_1 = g_2 = g_m$ = dc transconductance of the OTA. Hence, L is given by

$$L = \frac{C}{g_m^2} \tag{3}$$

Here, the electronically tuning capability of L can be achieved since g_m is electronically tunable by using the bias current of the OTA.

An example of the recently proposed OTA-based inductor is that in (Petchmaneelumka, 2009) which can be depicted as follows

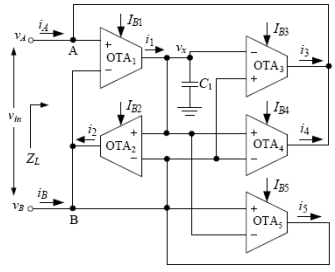

Figure 3 *A recently proposed OTA-based inductor in (Petchmaneelumka, 2009)*

This novel OTA-based inductor can realize the both positive and negative inductance without any topological changing since its L can be given by (Petchmaneelumka, 2009)

$$L = \frac{4V_T^2 C}{I_{B1} I_{B2}(1-K)} \tag{4}$$

where $K = I_{B4}/I_{B2} = I_{B5}/I_{B2}$ and V_T denotes the thermal voltage. Obviously, positive inductance can be obtained if and only if K<1 where as K>1 yields the negative inductance.Hence, this is electronically selectable via I_{B2}, I_{B4} and I_{B5}. Furthermore, the magnitude of L is electronically tunable via $I_{B1}$and K.

A major drawback of OTA-based inductor is that the high nonlinearity inherited from the OTA.

3.2 CCII-based inductor

A CCII-based inductor proposed in (Ferri et.al, 2003) will be discussed as an example. This active inductor can be depicted as follows.

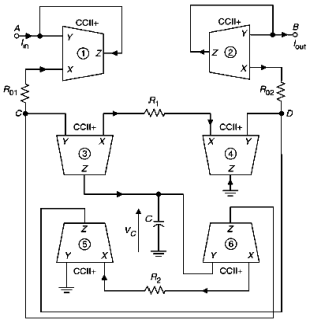

Figure 4 *CCII-based inductor in (Ferri et.al, 2003)*

Note that CCCIIs are also applicable to this circuit. Here, R_1 includes the contribution of the x-terminal parasitic resistances of CCII3 and CCII4 where as R_2 includes the contribution of the similar parasitic resistances of CCII5 and CCII6 (Ferri et.al, 2003). R_{o1} and R_{o2} denote the x-terminal parasitic resistance of CCII1 and CCII2 respectively. So, R_1, R_2, R_{o1} and R_{o2} are electronically adjustable via the bias currents of these CCIIs. The resulting L of this CCII-based inductor can be given by (Ferri et.al, 2003)

$$L = R_1 R_2 C \quad (5)$$

Obviously, L is electronically tunable due to the electronically tuning capabilities of parasitic resistances R_1 and R_2 mentioned above. However, such utilization the parasitic resistances which are conventionally undesired, is an important drawback.

3.3 CDBA-based inductor

Current Differencing Buffered Amplifier (CDBA) can also be used as the basis active element for the network level on-chip active inductor. As an example, a CDBA based inductor has been proposed in (Keskin, Hancioglu 2005). This circuit can be depicted as follows.

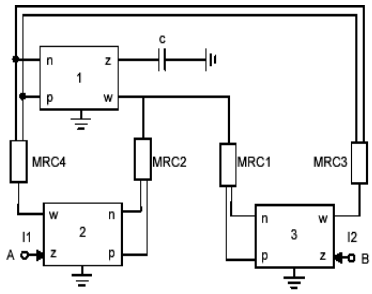

Figure 5 *CDBA based inductor* (*Keskin, Hancioglu 2005)*

It can be seen that the MOS Resistive Circuits (MRC) have been used as the intrinsic electronically tunable resistive elements. The internal structure of MRC is depicted below.

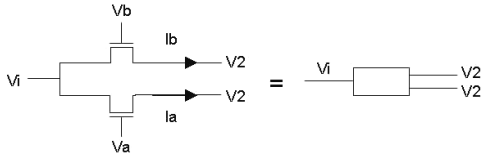

Figure 6 *Internal structure of MRC* (*Keskin, Hancioglu 2005)*

The conductance of the MRC can be electronically adjusted via V_a-V_b. The resulting L of this CDBA based inductor is given by

$$L = \frac{C}{(\mu C_{ox}(V_a - V_b))^2 \left(\frac{w}{l}\right)^2} \quad (6)$$

Obviously, L can also be electronically tuned via V_a-V_b. However, this CDBA based inductor requires the MRCs which must be in the triode region. Furthermore, this CDBA based inductor is not a compact one since several transistors are required for the implementation of CDBA.

3.4 Hybrid active inductor

The network level on-chip active inductor of this type contains more than one type of the active building blocks in the same circuit. For example, the hybrid on-chip active inductor which employed both OP-AMPs and Current Conveyors has been proposed in (Maundy et.al, 2007). This hybrid on-chip active inductor can be depicted as follows

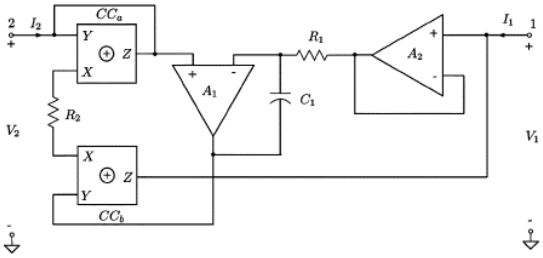

Figure 7 *Hybrid on-chip active inductor proposed in (Maundy et.al, 2007)*

By also using the OP-AMPs, the proposed hybrid on-chip active inductor gives higher Q-factor than those constructed by using only the Current Conveyors. The resulting L of this active inductor is given by

$$L = R_1 R_2 C_1 \quad (7)$$

Unfortunately, this L is not electronically tunable unless at least R_1, R_2 or C_1 is implemented by the electronically tunable element. Furthermore, both R_1 and R_2 are nominal passive resistors which consume considerably large chip area and power at the IC level.

4. Transistor Level Based On-Chip Active Inductors

A very classic example of the transistor level based on-chip active inductors is the CMOS active inductor proposed in (Thanachayanon, Payne, 1996) which can be depicted as follows

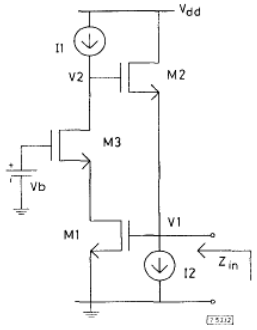

Figure 8 *CMOS active inductor in (Thanachayanon and Payne, 1996)*

This active inductor is constructed by using only three MOS transistors (not including biasing circuitry) without any nominal capacitance. Theoritically, it uses the gate-source capacitance (C_{gs}) which is the major parasitic capacitances of the MOS transistor as the capacitive load of the gyrator which composed of M1, M2 and M3. Basically, the gyrator can be realized by using only M1 and M2 but cascoding M3 to M1 reduces the inductor loss. By assumming identical transistors, L of this active inductor is approximately given by

$$L = \frac{C_{gs}}{g_m^2} \tag{8}$$

where g_m denotes the transconductance M1 and M2 which assumed to be identical. Obviously, electronically tuning capability of L can be obtained via the adjustment of g_m which is a function of the bias current.

Later, a modification has been made to the CMOS active inductor of (Thanachayanon, Payne, 1996) by simply adding the feedback resistor (R_f). This modification has been proposed in (Hsiao et.al, 2002) based on 0.18μm level. The resulting active inductor can be depicted in fig.9. Obviously, higher L and Q-factor can be obtained.

Similarly to its prototype, L of this active inductor can also be approximately given by (8) where g_m denotes the transconductance M1 and M3. The electronically tuning capability of L can also be obtained by a similar fashion. However, this on-chip active inductor requires R_f which is a troublesome passive resistor.

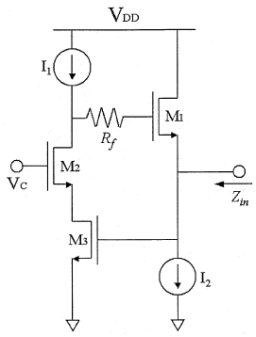

Figure 9 *On-chip active inductor in (Hsiao et.al, 2002)*

An all NMOS signal path on-chip active inductor has been proposed in (Xiao et.al, 2004) which can be depicted as follows

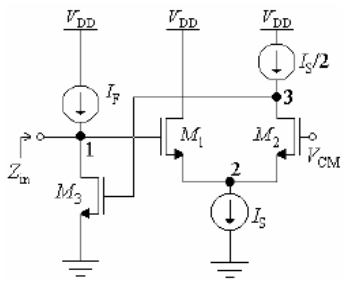

Figure 9 *On-chip active inductor proposed in (Xiao et.al, 2004)*

By using all NMOS in the signal path (M_1, M_2 and M_3) very high resonance frequency, f_R at GHZ level and very large Q-factor given practically by several hundred, can be obtained. Hence, this on-chip active inductor is applicable in the RF range. The gyrator is realized by M_1, M_2 and M_3 where as the total parasitic capacitance at node 3 (C_3) is used as the load. Since $g_{m1} = g_{m2}$ as M1 and M2 are

used as a transconductor within the gyrator, the resulting L can be given by (Xiao et.al, 2004)

$$L = \frac{2C_3}{g_{m1}g_{m3}} \quad (9)$$

Of course, electronically tuning capability of L can be obtained via the adjustment of g_{m1} and g_{m3} which depend on the corresponding bias currents.

The concept of source degeneration by capacitive element can be adopted for the improvement of the transistor level based on-chip active inductors. The result is entitled the CMOS Source Degenerated Differential Active Inductor (SDD-AI) which has been proposed in (Ler et.al, 2008) and can be depicted as follows

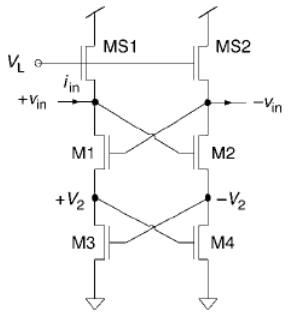

Figure 10 *The CMOS SDD-AI proposed in (Ler et.al, 2008)*

The SDD-AI is much more compact and simpler than the conventional active inductors. Furthermore, it has wider inductance tuning range and higher f_R. M1 and M2 are used as the differential mode gyrator where as M3 and M4 give the capacitive source degenerations to M1 and M2 respectively. MS1 and MS2 serve as the stabilisers.

By assumming that the SDD-AI is perfectly symmetrical, L can be derived by using the half circuit analysis as follows (Ler et.al, 2008)

$$L = \frac{C_{gs1} + C_{v2}}{g_{m1}^2} \quad (10)$$

where C_{v2} denotes the total parasitic capacitance at node v_2. The electronically tuning capability of L can be obtained by tuning the bias current of M1 which controls g_{m1}.

By the careful comparison of (8)-(10), it can be seen that the recenly proposed active inductor for example those in (Xiao et.al, 2004) and (Ler et.al, 2008) give higher value of L than the classical one in (Thanachayanon, Payne, 1996) with the similar level technology and other conditions assumed.

Conventionally, the Q-factor of a typical CMOS on-chip active inductor is dependent upon the signal swing at the input as proposed in (Tang et.al, 2009). This input signal swing dependent Q-factor is denoted by $Q(\omega_0,I)$ where ω_0 and I denote the operating frequency and input signal in the form of input current of the active inductor respectively (Tang et.al, 2009). As such, a better figure of merit entitled mean Q-factor ($Q_m(\omega_0)$) which equivalents to the average of $Q(\omega_0,I)$ over the entire range of the input current swing given by I_{min} to I_{max}, is introduced in (Tang et.al, 2009) as

$$Q_m(\omega_o) = \frac{1}{I_{max} - I_{min}} \int_{I_{min}}^{I_{max}} Q(\omega_o, J)dJ \quad (11)$$

where J denotes the input current in term of the integrating variable.

Also in (Tang et.al, 2009), an on-chip active inductor with the constant Q-factor with respect to the input current swing has been proposed which can be depicted in fig. 11. It can be seen that this constant Q-factor active inductor can be simply derived from the current reuse active inductor previously proposed in (Wu et.al, 2001) which is shown in the shaded area of fig. 11. This can be done by simply adding the current feedback network which is composed of M_3-M_7 and J_2.

As a result, I_{D2} is approximately fixed at the maximum value of the input current. So, the change

in g_{m2} which is a function of I_{D2}, with respected to the input current swing is minimized. As such, the similar changes in both L and Q-factor are also minimized since both quantities are functions of g_{m2}. Hence, an active inductor with input current swing independent Q-factor can be obtained. However, this achievement can be accomplished if and only if

$$k_1 k_2 k_3 \gg 1 \quad (12)$$

where k_1, k_2 and k_3 denote the current gain of the current mirror M2-M3, M4-M5 and M6-M7. So, it can be seen that the current mirrors with considerably large current gains are necessary.

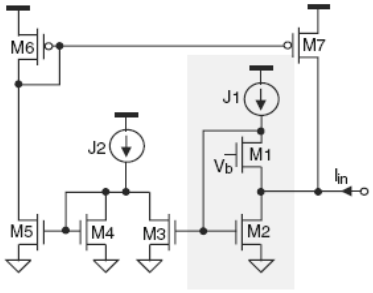

Figure 11 *Constant Q-factor on-chip active inductor in (Tang et.al, 2009)*

5. Discussion: Comparison of Network Level and Transistor level Based On-Chip Active Inductor

Obviously, the network level based on-chip active inductors require more amount of the power consumption and chip area than the transistor level based ones. They also generate more noise. These are because a typical network level based on-chip active inductor contains larger number of transistors than a transistor level based one. Hence, the transistor level based active inductors are strongly recommended for the extremely low power/low noise applications

However, the network level based on-chip active inductors are additionally able to operate in the kHz-a few MHz range unlike their transistor level based counterparts which most of them are able to operate only within much higher ranges for example the microwave and RF range. This is because the network level based on-chip active inductors use the nominal capacitances which their effects exist for all frequency ranges, as the capacitive load where as the transistor level based ones use the parasitic capacitances for example C_{gs} which their effects become significant only within very high frequency ranges in order to do so.

Furthermore, the network level based active inductors are less suffered by the parasitic elements since the nominal capacitances are much larger than the parasitic ones. In the other words, the effects of the parasitic capacitances can be abosorbed. According to these reasons, the network level based active inductors are strongly recommended for those applications which the operating bandwidths include those frequencies within kHz-a few MHz range and those applications which the parasitic effects cannot be tolerated.

6. Conclusion

Many recent microelectronic applications require the usage of the on-chip inductors. The on-chip active inductors which have many advantages over the passive ones have been found to be the promising replacements. This paper focuses on the overview of the on-chip active inductors. The fundamental concept has been firstly mentioned followed some examples of both network level and transistor level based on-chip active inductors. Finally, the comparison between the on-chip active inductors of both categories has been discussed. This paper should be useful for those who interest in the design and development of any applications involving on-chip active inductors.

7. Acknowledgement

The author would like to acknowledge Mahidol University, Thailand for the online database service.

8. Referrences

Chen, J., Liou, J.J. (2004). On-chip spiral inductors for RF applications: an overview, *Journal of Semiconductor Technology and Science*, Vol 4, No. 3, 149-167.

Green, M.M. (1996). On Power Transmission of LC Ladder Filters using Active Inductor Realizations, *IEEE Transactions on Circuits and Systems-I,* Vol. 43, No.6, 509-511.

Singer, S. (1988). Loss-Free Gyrator Realization, *IEEE Transactions on Circuits and Systems*, Vol. 35, No.1, 26-34.

Banchuin, R., Chipipop. B., Sirinaovakul, B. (2008), Novel conventional standard linear element based complete passive equivalent circuit model of the practical OTA-based inductors, *IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences*, Vol. E91-A, No.8, 1883-1889.

Geiger, R.L., Sanchez-Sinencio, E. (1985), Active filter design using Operational Transconductance Amplifiers: a tutorial, *IEEE Circuits and Devices Magazines*, Vol.1, 20-32.

W. Petchmaneelumka. (2009), *OTAs-based positive/negative floating inductance smulator,* Proceedings of the International MultiConference of Engineers and Computer Scientists 2009, Hongkong, March 18-20.

Ferri, G., Guerrini, N.C., Diqual, M. (2003), CCII-based floating inductance simulator with compensated series resistance, *Electronics Letter*, Vol.39.

Keskin, A.U., Hancioglu, E. (2005), CDBA-based synthetic floating inductance circuits with electronic tuning properties, *ETRI Journal*, Vol.27, No.2, 239-242.

Maundy, B., Gift, S., Aronhime, P. (2007), A novel hybrid active inductor, *IEEE Transactions on Circuits and Systems—II: Express Brief*, Vol. 54, No. 8, 663-667.

Thanachayanon, A., Payne, A. (1996), VHF CMOS integrated active inductor, *Electronic Letters*, Vol.32, 999-1000.

Hsiao, C.C. Kuo CW., Ho, CC. Chan, YJ. (2002), Improved quality-factor of 0.18-μm CMOS active inductor by a feedback resistance design, *Microwave and Wireless Components Letters*, Vol.12, 467 – 469.

H. Xiao, R. Schaumann, W. Robert Daasch, P.K. Wong and B. Pejcinovic (2004), *A Radio-Frequency CMOS Acitve Inductor and Its Applications in Designing High-Q Filters*, Proceedings of the IEEE International Symposium on Circuits and Systems 2004, Vancouver, Canada, May 23-26.

Ler, C.L., A'ain, A.K.B., Kordesh, V. (2008), CMOS source degenerated differential active inductor, *Electronic Letters*, Vol.44, No 3.

Tang, A., Yuan, F., Law, E. (2009), A new constant-Q CMOS active inductor with applications to low-noise oscillators, *Analog Integrated Circuits and Signal Processing-: Mixed Signal Letter,* Vol.58, No.1, 77-80

Wu, Y., Ismail, M., Olsson, H. (2001), CMOS VHF/RF CCO based on active inductors, *Electronic Letters*, Vol.37, No.8, 472-473.