A Novel Design of Adaptively Biased Linear MOS Transconductor

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Abstract : This paper presents a new circuit for linear MOS operating transconductance amplifier (OTA). A proposed OTA based on a source-coupled pair which is linearized by a new adaptive biasing circuit. A conventional adaptively biased MOS transconductor is known as a linear OTA. However, the OTA is necessary to employ a single-end converter circuit in order to realize linear transfer characteristics, and it has low PSRR. In this paper, a new adaptively biased OTA has good linearity without a single-end converter circuit and high PSRR is proposed. Simulation results show that the proposed OTA is effective for improvement of the linearity, PSRR, CMRR and THD.

Keywords: CMOS, Analog Integrated Circuits, Linear Circuits, Adaptively Biased MOS Transconductors

1. Introduction

The MOS operating transconductance amplifier (OTA) is a fundamental building block for analog signal processing circuits, such as filters and multipliers. The transfer characteristic is desired to be linear.

An adaptively biased OTA is known as linear OTA. However, the conventional adaptively biased OTA [1] has low the power supply rejection ratio (PSRR) due to receive influence by change of the power supply easily. Moreover, the linearity of the conventional OTA is realized by using a single-end converter circuit. If the output current is removed from each of the output terminal, the linearity cannot be achieved. Therefore, the conventional OTA is not available to apply to the filter, etc. Another type of OTA, a bias offset transcondactor [2][3] is known as a linear OTA. The size of OTA become large due to the operating OTA is necessary to employ a floating voltage source.

In this paper, a new adaptively biased linear MOS OTA is proposed. The proposed OTA has high PSRR and linear transfer characteristics without the single-end converter circuit. Explaining the idea concretely, The liner transfer characteristics and the high PSRR are realized by using the new adaptively biasing circuit to eliminating the second-order term of the input voltage that it is the cause of nonlinearity of OTA [4][5]. Moreover, even if the output current is removed from each of the output terminal, the linear transfer characteristic of the proposed OTA is obtained. Simulation results show that the proposed circuit is effective for improvement of the linearity, PSRR, CMRR and THD.

2. Conventional adaptively biased OTA

Fig.1 shows a basic building circuit for the adaptively biased OTA.

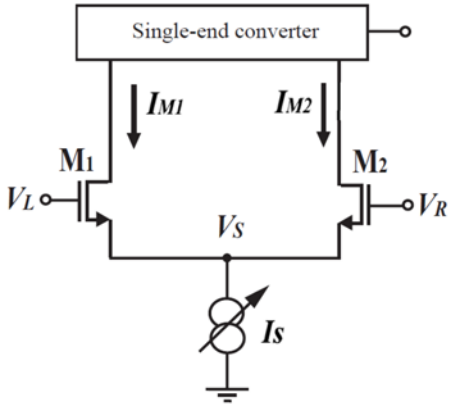


Figure 1 Basic configuration of adaptively biased OTA

Assuming that the overall of transistor operate in saturation region, the drain current of MOSFETs obeys the square-law characteristic. The drain current of M1, M2, and the tail current IS are expressed as

$$I_{M1} = K_N(V_L - V_S - V_T)^2$$
$$I_{M2} = K_N(V_R - V_S - V_T)^2$$
$$I_S = I_{M1} + I_{M2} \quad (1)$$

where KN is the transconductance factor, VT is the threshold voltage, and VS is the common-source voltage of M1 and M2, respectively. Assuming that the input voltages are fully differential signals, VL and VR are expressed as

$$V_L = \frac{1}{2}V_{in}$$
$$V_R = -\frac{1}{2}V_{in} \quad (2)$$

From solving (1) and (2), the common source voltage VS is obtained as

$$V_S = -\frac{\sqrt{2K_N I_S - K_N^2 V_{in}^2}}{2K_N} - V_T \quad (3)$$

According to (1) and (3), the large-signal behavior of the single-ended output current Iout (Iout = IM1 - IM2) is expressed as

$$I_{out} = V_{in}\sqrt{K_N(2I_S - K_N V_{in}^2)} \quad (4)$$

where I_S is the tail current that is realized by the adaptively biasing circuit. If the adaptively biased circuit can eliminate the second-order nonlinear term of the input voltage that exist in the transfer function, the transfer characteristic of OTA become linear [4][5].

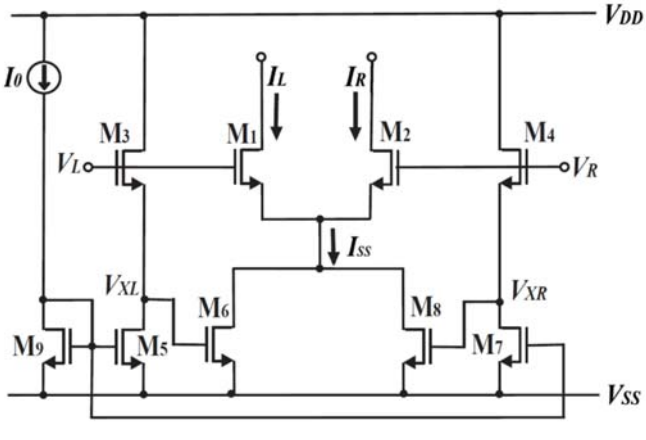


Figure 2 Conventional adaptively biased OTA

Fig.2 shows the conventional adaptively biased linear OTA (namely Susanta OTA) [1] that is realized by using the linearization technique ahead. In this OTA, the drain current of M6 and M8 are expressed as

$$I_{M6} = K_N(\frac{V_{in}}{2} - \sqrt{\frac{I_0}{K_N}} - 2V_T - V_{SS})^2 \ 2$$
$$I_{M8} = K_N(-\frac{V_{in}}{2} - \sqrt{\frac{I_0}{K_N}} - 2V_T - V_{SS})^2 \quad (5)$$

where VSS is the common-source voltage of M1 and M2 of the circuit in Fig.2. According to (5), the current I_{SS} ($I_{SS} = I_{M6} + I_{M8}$) is expressed as

$$I_{SS} = 2K_N(\sqrt{\frac{I_0}{K_N}} + 2V_T + V_{SS})^2 + \frac{K_N V_{in}^2}{2} \quad (6)$$

When (5) is substituted for (4), the output current Iout and the transconductance Gm of the Susanta OTA are obtained as

$$I_{out} = 2K_N V_{in}(\sqrt{\frac{I_0}{K_N}} + 2V_T + V_{SS}) \quad (7)$$

$$G_m = 2K_N(\sqrt{\frac{I_0}{K_N}} + 2V_T + V_{SS}) \quad (8)$$

According to (7) and (8), we can see that the transfer characteristic of Susanta OTA is linear. However, PSRR become low due to the supply voltage VSS exists in the transfer function. In the next section, we propose a new adaptively biased linear MOS OTA that has high PSPP.

3. Proposed OTA

3.1 Improving high PSRR

Fig.3 shows a proposed high PSRR of the new adaptively biased linear MOS OTA configuration. In order to improve the linearity of the proposed OTA, the aspect ratio of M8, M10 versus M7, M9 are set as **α**, respectively.

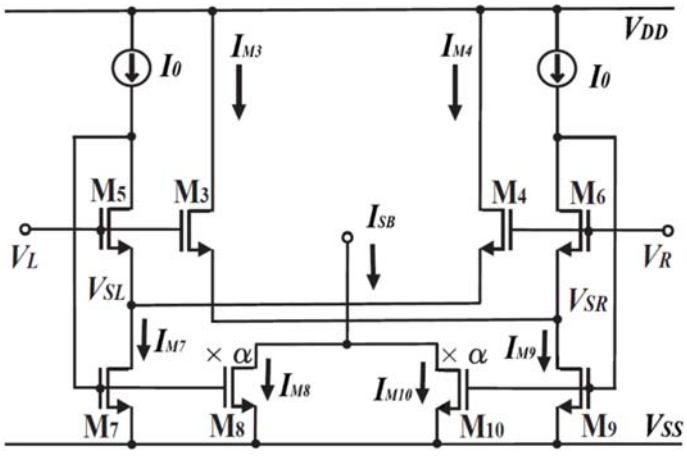


Figure 3 Adaptively biasing circuit design for improvement of PSRR

The drain current of M7 and M9 are expressed as

$$I_{M7} = K_N V_{in}^2 - 2\sqrt{I_0 K_N} V_{in} + 2I_0$$
$$I_{M9} = K_N V_{in}^2 + 2\sqrt{I_0 K_N} V_{in} + 2I_0 \quad . \qquad (9)$$

From (9), because the current amplification factor is set as α, the current ISB that connected to the tail current of the circuit in Fig.1 is expressed as

$$I_{SB} = \alpha(I_{M7} + I_{M9}) = \alpha\left(2K_N {V_{in}}^2 + 4I_0\right) \quad . \quad (10)$$

From (3) and (10), improving the linearity of the proposed OTA, the second-order nonlinear term of the input voltage Vin in (3) is eliminated by (10). Solving these relations, the aspect ratio α is obtained as α=1/4. Therefore, the large-signal behavior of the single-ended output current Iout and the transconductance Gm are expressed as

$$I_{out} = \sqrt{2K_N I_0} V_{in}$$
$$G_m = \sqrt{2K_N I_0} \qquad (11)$$

According to (11), we can see that the transfer characteristic of the proposed OTA is linear and the PSRR is improved. Therefore, the new adaptively biased linear OTA with high PSRR is achieved.

3.2 Linear OTA without single-end converter circuit From (11), the linear transfer characteristic of the proposed OTA configuration in Fig.3 is obtained by using the single-end converter circuit (Iout = IM1 - IM2). If the output current is achieved without using the singleend converter circuit, the drain current of M1 and M2 are obtained as

$$I_{M1} = K_N\left(\frac{V_{in}}{2} + \sqrt{\frac{I_0}{2K_N}}\right)^2$$
$$I_{M2} = K_N\left(-\frac{V_{in}}{2} + \sqrt{\frac{I_0}{2K_N}}\right)^2 \qquad (12)$$

The second-order nonlinear term of the input voltage exists in the current function IM1 and IM2. Therefore, we can see that the linearity cannot be achieved when the output current is removed from each of the output terminal. That is not available to apply to the filter, etc.

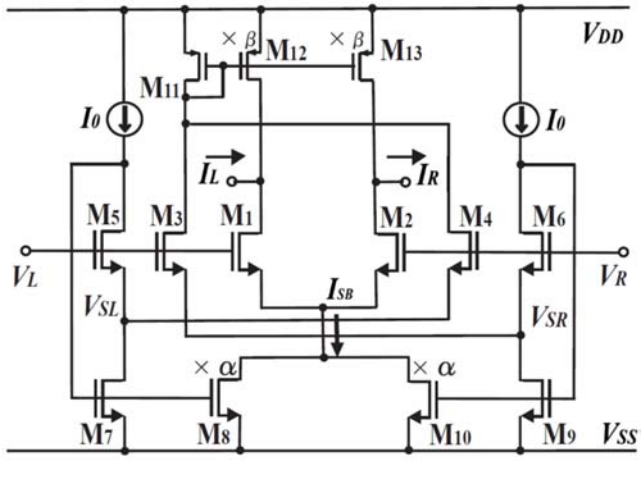


Figure 4 Proposed OTA

Fig.4 shows the proposed OTA that improve the drawback of circuit shown in Fig.3. In the proposed OTA, the drain terminal of M4 is connected to the drain terminal of M3. Then, the overall drain current of M3, M4 is used to eliminate the nonlinear term of (12). In order to improve the linearity, the current amplification of the current mirror (M11–M13) is set as β. The drain current of M3 and M4 are expressed as

$$I_{M3} = K_N(\sqrt{\frac{I_0}{K_N}} + V_{in})^2$$
$$I_{M4} = K_N(\sqrt{\frac{I_0}{K_N}} - V_{in})^2 \quad (13)$$

The drain current of M12 and M13 are obtained as

$$I_{M12} = I_{M13} = \beta(2K_N V_{in}^2 + 2I_0) \quad . \quad (14)$$

From (12), (14), Solving the equation of IM1 = IM12 and IM2 = IM13, the current amplification of the current mirror M11–M13 is obtained as β=1/8. The output currents IL, IR each of the output terminal are given as

$$I_L = I_{M1} - I_{M12}$$
$$I_R = I_{M13} - I_{M2} \quad (15)$$

Solving (15), the output current IL, IR each of the output terminal are obtained as

$$I_L = I_R = \sqrt{K_N I_0}\, V_{in} \quad (16)$$

According to (16), we can see that the linearity of the proposed OTA is improved when the output currents are removed from each of the output terminal. Therefore, the new adaptively biased linear MOS OTA that has high PSRR and good linear transfer characteristics without the single-end converter circuit has been achieved.

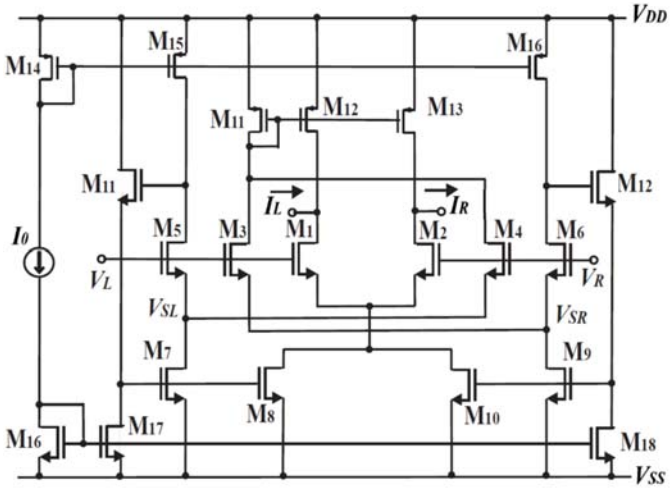


Figure 5 Proposed OTA configuration for simulation

4. Simulation

In order to confirm the effective of the proposed OTA, simulation was carried out. The used program software is SIMetrix. In simulation, 0.18μm BSIM3 model is used. The supple voltage is ±0.9 V. The proposed OTA used for simulation is shown in Fig.5. The optimum aspect ratios of α and β are set as 1/4 and 1/8, respectively. Size of each transistors are shown in Table 1.

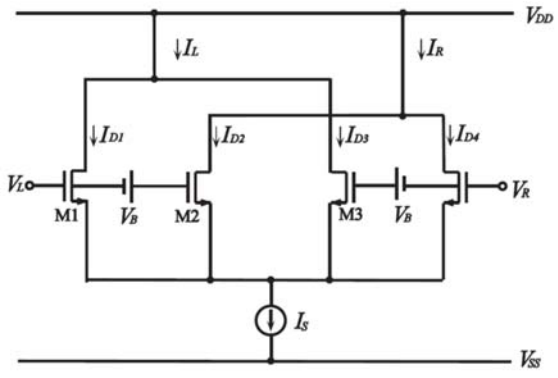


Figure 6 Linear MOS OTA using bias-offset technique

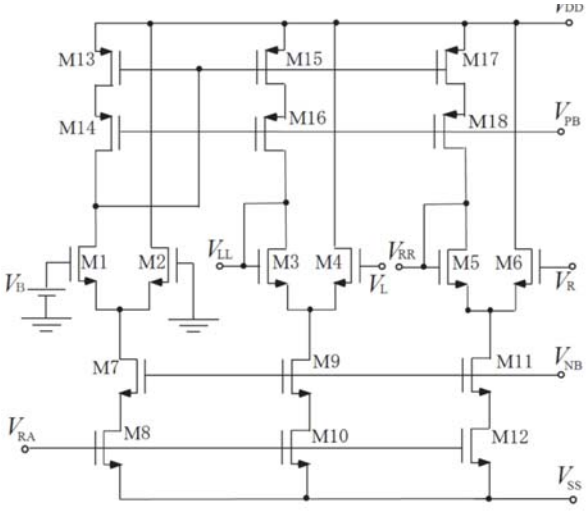


Figure 7 Floating voltage source

4.1 Comparison with other OTA

A bias offset OTA shown in Fig.6 is used as the comparison OTA. The transconductance is expressed as

$$G_m = 2K_N V_B \tag{17}$$

According to (17), we can see that the bias off set OTA is a linear OTA. However, Operating the OTA, the supply bias voltage VB is a must. The floating voltage source that achieves the supply bias voltage VB is shown is Fig.7.

Table 1 Size of transistors

Transistors	*W/L*
M1, M2, M3, M4, M5, M6	1.8μm/1.8μm
M7, M9	27μm/1.8μm
M8, M10	6.75μm/1.8μm
M11	16μm/1.8μm
M12, M13	2μm/1.8μm
M14, M15, M16	18μm/1.8μm

4.2 Gm characteristics

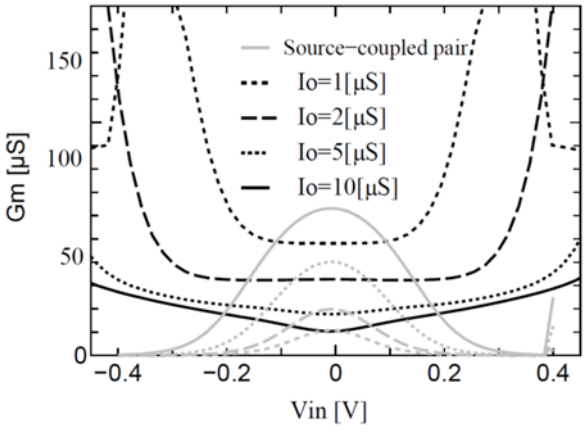
Fig.8 (a) illustrates Gm characteristics of the proposed OTA and the differential pair for various operating current. According to Fig.8 (a), we can see that even if the operating current is changed, the linearity of the proposed OTA almost flattens in the input range. Moreover, Fig.8 (b) illustrates the normalized Gm characteristics (Gm/Gm(0)) for each of compared OTAs when the operating current is set as 5μA. In order to compare the linearity, the transconductance error Gmer [%] for each of OTAs is shown in Table 2. The Gmer[%] is defined as

$$G_{mer} = \left(\frac{G_{mmax} - G_{mmin}}{G_m(0)}\right) \times 100 \tag{18}$$

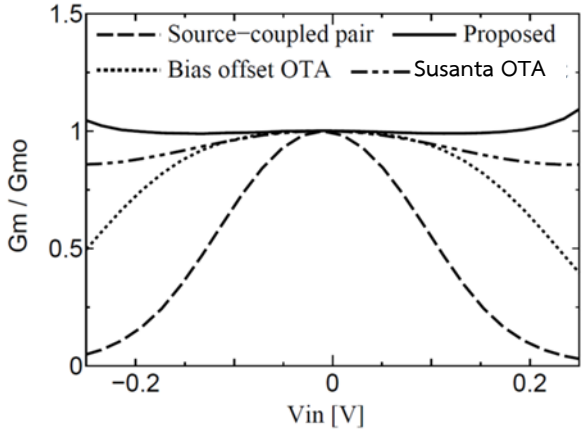
where G_{mmax} and G_{mmin} are the maximum G_m and the minimum Gm in the input range, respectively. $G_m(0)$ is the *Gm* at V_{in} = 0 V. The input voltage range is ±0.2 V. From Fig.8, we can see that the linearity of the proposed OTA is better than the compared OTAs.

Table 2 Gmer [%] for each circuit

OTAs	G_{mer}
Proposed OTA	0.22 %
Susanta OTA	11.7 %
Bias-offset OTA	25.3 %
Source-coupled pair	83.5%



(a) G_m of Proposed OTA and differential pair



(b) G_m of compared OTAs

Figure 8 Gm characteristics

4.3 Frequency characteristics

Fig.9 illustrate the power supply rejection ratio (PSRR) of the proposed OTA and Susanta OTA. From the simulation result, it should be noticed that PSRR of the proposed OTA is improved as the theoretical computation. The common mode rejection ratio (CMRR) for each of OTAs is plotted in Fig.10. From Fig.10, we can see that the CMRR of the proposed OTA is higher than other compared OTAs.

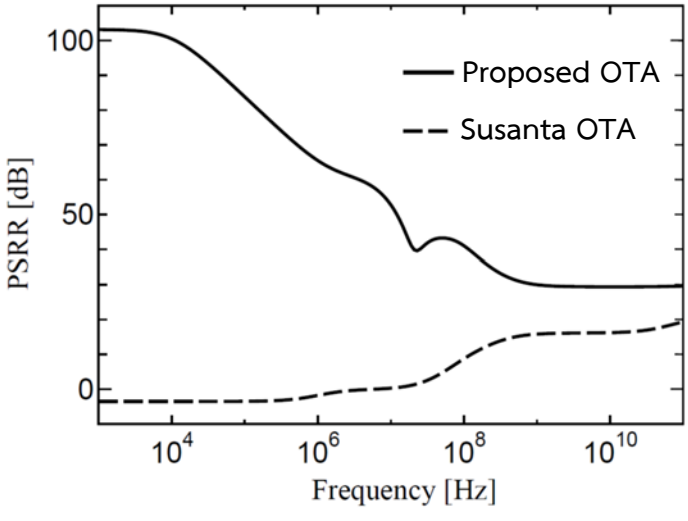


Figure 9 Power Supply Rejection Ratio (PSRR)

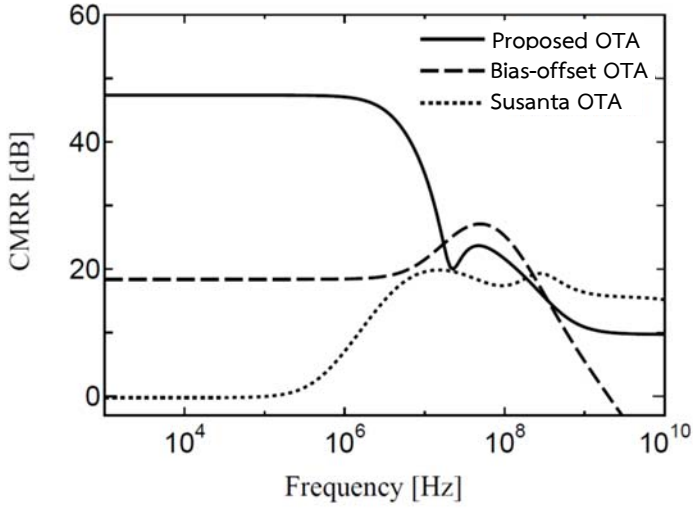


Figure 10 Common Mode Rejection Ratio (CMRR)

4.4 Total harmonic distortion

The total harmonic distortion (THD) of the output differential current versus the amplitude of the input voltage for the proposed OTA and the Susanta OTA is plotted in Fig.11. The sinusoidal input is 1MHz. and the input signal amplitude is 0.1V – 0.4V. This figure shows that the THD of the proposed OTA is lower that the Susanta OTA.

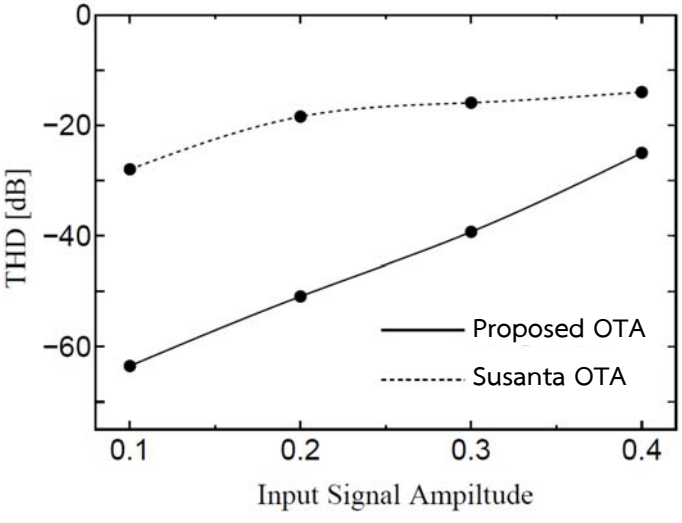


Figure 11 Total harmonic distortion (THD) for 0.1 – 0.4 V amplitude input, 1MHz sinusoidal input

5. Conclusion

A new adaptively biased linear MOS OTA has been present. The linearity and the high PSRR are realized by using the new adaptively biased circuit to eliminating the second-order nonlinearity term of the differential pair. Moreover, even if the output current of the proposed OTA is removed from each of the output terminal, the linear transfer characteristic is obtained. Simulation results show the proposed OTA has good linearity and lower CMRR, PSRR, THD compared to other OTAs.

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7. References

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