An Adaptively Biased Linear MOS Transconductor for Low Power Application

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Abstract : An adaptively biased linear MOS transconductor is known as a linear transconductor. However, if the low transconductance is needed, small operating current makes MOSFETs operate in weak inversion. In this case, the voltage-current characteristic is not expressed as a square-law characteristic but is expressed as an exponential function. Thus, the factor makes linearity of the transconductor worse. In this paper, a new design of the adaptively biased linear MOS transconductor considering the influence of MOSFETs operating in weak inversion is proposed. In the proposed technique, an adaptive biasing circuit is newly designed for improvement of the linearity deterioration. Simulation results show that the proposed technique is effective for improvement of the linearity.

Keywords : CMOS, Analog Integrated Circuits, Linear Circuits, Adaptively Biased MOS Transconductors

1. Introduction

A transconductor is a circuit to convert input signal voltages into signal currents. The voltage-current characteristic is desired to be linear. However, the linearity is deteriorated by non-ideal factors.

An adaptively biased linear MOS transconductor [1] is known as a linear transconductor. The good linearity is realized by subtraction of individual differential output currents using single-end converter. However, the transconductor has drawbacks; 1) the power supply rejection ratio (PSRR) and the common mode rejection ratio (CMRR) are low and 2) the linearity is not realized if the output currents are taken out from each of differential output terminals, namely the individual differential output currents are not linear. For improvement of the drawbacks, an adaptively biased linear MOS transconductor composed of a square current source and a differential pair [2] has been already proposed. The transconductor has good properties, such as high PSRR, high CMRR, and good linearity of the individual differential output currents. However, if the low transconductance for low power applications is needed such as biomedical devices, low operating current makes MOSFETs operate in weak inversion. In this case, the voltage-current characteristic is not expressed as a square-law characteristic but is expressed as an exponential function [5][6]. Thus, the factor makes linearity of the transconductor worse.

In this paper, a new design of adaptively biased linear MOS transconductor considering the influence of MOSFETs operating in weak inversion is proposed. In the proposed technique, an adaptive biasing circuit is newly designed for improvement of the linearity deterioration. Simulation results show that the proposed technique is effective for improvement of the linearity.

2. Principle of differential input/output transconductor

Fig.1(a) shows a basic configuration of the single-ended type of adaptively biased linear MOS transconductor. Assuming that MOSFETs operate in saturation region and the drain currents obey the square-law characteristic, the drain currents of M1, M2, and the tail current IS are expressed as

$$\begin{aligned} I_{M1} &= K_N(V_L - V_S - V_T)^2 \\ I_{M2} &= K_N(V_R - V_S - V_T)^2 \\ I_S &= I_{M1} + I_{M2} \ , \end{aligned} \tag{1}$$

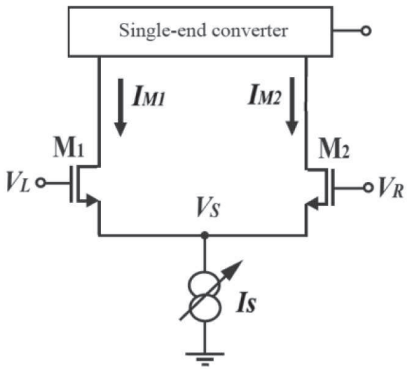
where K_N is the transconductance factor, V_T is the threshold voltage, and V_S is the common source voltage of M1 and M2. Assuming that the input voltages are fully differential signals, V_L and V_R are expressed as

$$\begin{aligned} V_L &= \frac{1}{2}V_{in} \\ V_R &= -\frac{1}{2}V_{in} \ . \end{aligned} \tag{2}$$

From (1) and (2), the source voltage V_S is expressed as

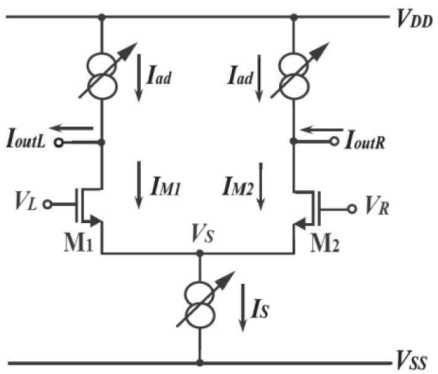
$$V_S = \frac{\sqrt{2K_N I_S - K_N{}^2 V_{in}{}^2}}{2K_N} - V_T \ . \quad (3)$$

(a)



(a) Single-ended type

(b)



(b) Differential input/output type

Fig.1 Basic Configulation of Adaptively Biased Linear MOS Transconductor (a) Single-ended Type, (b) Differential Input/output Type

It is seen from (3) that the source voltage VS is a function of the input voltage Vin. For linearization, VS has to be set to constant. Therefore, the tail current IS is expressed as

$$I_S = \frac{K_N V_{in}{}^2}{2} + A \ , \quad (4)$$

where A is a constant. From (1) – (4), the single-ended output current is expressed as

$$I_{out} = I_{M1} - I_{M2} = \sqrt{2K_N A}\, V_{in} \ . \quad (5)$$

It is seen from (5) that linearity of the transfer characteristic with single-end conversion is achieved. The circuit design using this technique has been reported in the paper [3, 4]. However, in case of the individual differential output terminals are needed, the individual differential output currents are obtained as

$$I_{M1} = \frac{K_N V_{in}{}^2}{4} - \sqrt{\frac{AK_N}{2}} V_{in} + \frac{A}{2}$$
$$I_{M2} = \frac{K_N V_{in}{}^2}{4} + \sqrt{\frac{AK_N}{2}} V_{in} + \frac{A}{2} \ . \quad (6)$$

It should be noticed from (6) that the individual differential output currents are quadratic function of the input voltage. This means that the linearity of individual differential output terminals cannot be achieved using the basic configuration shown in Fig1(a).

Fig.1(b) shows a basic configuration of the differential input/output type of adaptively biased linear MOS transconductor. In Fig.1(b), the individual differential output currents I_{outL} and I_{outR} are given by

$$\begin{aligned} I_{outL} &= I_{ad} - I_{M1} \\ &= I_{ad} - \frac{K_N {V_{in}}^2}{4} + \sqrt{\frac{AK_N}{2}} V_{in} - \frac{A}{2} \\ I_{outR} &= I_{M2} - I_{ad} \\ &= -I_{ad} + \frac{K_N {V_{in}}^2}{4} + \sqrt{\frac{AK_N}{2}} V_{in} + \frac{A}{2}, \end{aligned} \quad (7)$$

where Iad is the bias current for linearization IoutL and IoutR. In order to eliminate the nonlinear term, the bias current Iad is expressed as

$$I_{ad} = \frac{K_N {V_{in}}^2}{4} + \frac{A}{2} \ . \quad (8)$$

Substituting (8) into (7), I_{outL} and I_{outR} are expressed as

$$I_{outL} = I_{outR} = \sqrt{\frac{AK_N}{2}} V_{in} \ . \quad (9)$$

It is seen from (9) that the differential input/output linear transconductor is achieved using the basic configuration shown in Fig.1(b). A circuit design using this technique is described in the next section.

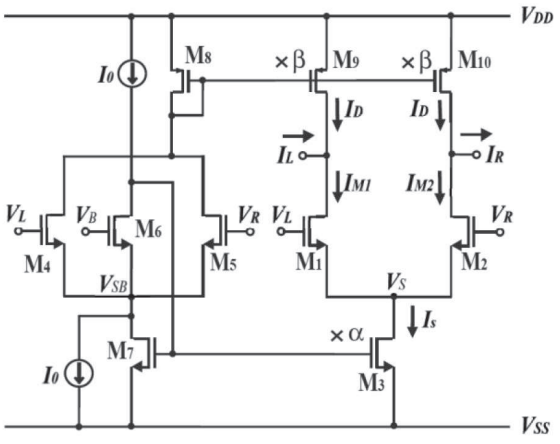


Fig.2 Conventional transconductor

3. Circuit design of differential input/output transconductor

Fig.2 shows the adaptively biased linear MOS transconductor [2] using the technique described in section 2. In Fig.2, M1 and M2 compose a differential pair, M4 – M6 and the operating current I0 compose a square current source. The current mirror composed of M3 and M7 supplies the tail current IS , whose current amplification factor is set to α = 1. The current mirror composed of M8 – M10 supplies the bias current ID, whose current amplification factor is set to β = 1/2. The drain currents of M4 – M6 are expressed as

$$\begin{aligned} I_{M4} &= K_N (V_L - V_{SB} - V_T)^2 \\ I_{M5} &= K_N (V_R - V_{SB} - V_T)^2 \\ I_{M6} &= I_0 = K_N (V_B - V_{SB} - V_T)^2 \ , \end{aligned} \quad (10)$$

where V_{SB} is the common source voltage of M4 – M6. The bias voltage V_B is realized by a simple active voltage divider, and is given by

$$V_B = \frac{1}{2}(V_L + V_R) = 0 \ . \quad (11)$$

From (10) and (11), V_{SB} is expressed as

$$V_{SB} = -\sqrt{\frac{I_0}{K_N}} - V_T \ . \quad (12)$$

The drain currents of M7 and M8 are given by

$$I_{M7} = I_{M4} + I_{M5} + I_{M6} - I_0 \quad (13)$$
$$I_{M8} = I_{M4} + I_{M5} \ .$$

From (10) – (13), IS and Iad are expressed as

$$I_{M3} = I_S = \frac{K_N {V_{in}}^2}{2} + 2I_0 \quad (14)$$
$$I_{M9,10} = I_{ad} = \frac{K_N {V_{in}}^2}{4} + I_0 \ .$$

From (7) and (14), the individual differential output currents are expressed as

$$I_{outL} = I_{outR} = \sqrt{I_0 K_N} V_{in} \ . \quad (15)$$

It is seen from (15) that the transfer characteristics of the transconductor are linear.

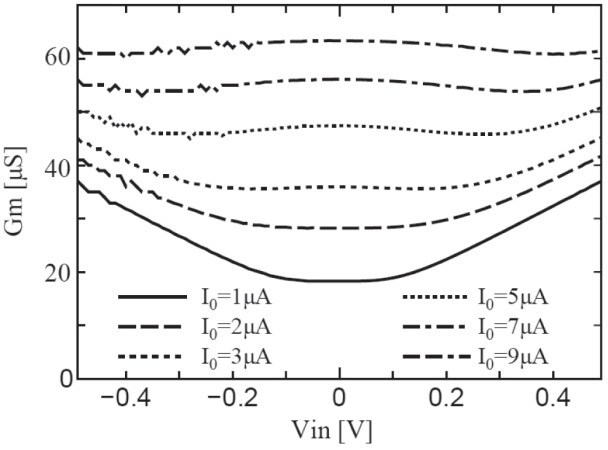


Fig.3 Transconductance Characteristics

Fig.3 illustrates simulation result of the transconductance characteristics for various operation currents of the transconductor shown in Fig.2. Fig.3 shows that if the operating current is small, e.g. I_0 = 1μA – 3μA, the transconductance characteristics are not flat. The deterioration is caused mainly by two cores of differential pairs M1 – M2 and M4 – M5 operating in weak inversion. Thus, the drain currents is not expressed as the square-law characteristic but is expressed as the exponential function [5][6]. Assuming that M1 – M2 and M4 – M5 operate in weak inversion, the drain currents are expressed as

$$I_{M1} = I_{D0} \exp\left(\frac{V_L - V_S - V_T}{nU_T}\right)$$
$$I_{M2} = I_{D0} \exp\left(\frac{V_R - V_S - V_T}{nU_T}\right)$$
$$I_{M4} = I_{D0} \exp\left(\frac{V_L - V_{SB} - V_T}{nU_T}\right)$$
$$I_{M5} = I_{D0} \exp\left(\frac{V_R - V_{SB} - V_T}{nU_T}\right) \ , \quad (16)$$

where I_{D0} is the reverse saturation current, n is the subthreshold slope factor, and $U_T = kT/q$ is the thermal voltage that k is the Boltzmann's constant, T is the absolute temperature and q is the electronic charge [5][6]. From (2), (12), and (16), the tail current I_S realized by the square current source is expressed as

$$I_S = I_{D0}\left(1 + \exp\left(\frac{V_{in}}{nU_T}\right)\right) \exp\left(\frac{-2\sqrt{I_0/K_N} + V_{in}}{2nU_T}\right). \quad (17)$$

From eqs. (2) and (16), the source voltage V_S is expressed as

$$V_S = \frac{V_{in}}{2} - V_T + nU_T \log\left(\frac{I_{D0}\left(1+\exp\left(\frac{-V_{in}}{2}\right)\right)}{I_S}\right). \quad (18)$$

Substituting eqs. (17), (18) is rewritten as

$$V_S = \frac{V_{in}}{2} - V_T + nU_T \log\left[\exp\left(-\frac{2\sqrt{I_0/K_N}+V_{in}}{2nU_T}\right)\right]. \quad (19)$$

From eq. (19), IM1 and IM2 are rewritten as

$$I_{M1} = I_{D0}\exp\left(\frac{2\sqrt{I_0/K_N}+V_{in}}{2nU_T}\right)$$
$$I_{M2} = I_{D0}\exp\left(\frac{2\sqrt{I_0/K_N}-V_{in}}{2nU_T}\right). \quad (20)$$

The output current is expressed as

$$I_{out} = I_{D0}\left(\exp\left(\frac{V_{in}}{2nU_T}\right)-1\right)\exp\left(\frac{2\sqrt{I_0/K_N}-V_{in}}{2nU_T}\right). \quad (21)$$

The transconductance is expressed as

$$G_m = \frac{I_{D0}}{2nU_T}\left(\exp\left(\frac{V_{in}}{nU_T}\right)+1\right)\exp\left(\frac{2\sqrt{I_0/K_N}-V_{in}}{2nU_T}\right). \quad (22)$$

It is found from eq. (22) that the transconductance is not flat due to MOSFETs operating in weak inversion, as shown in Fig.3. A technique to alleviate this problem is described in the next section.

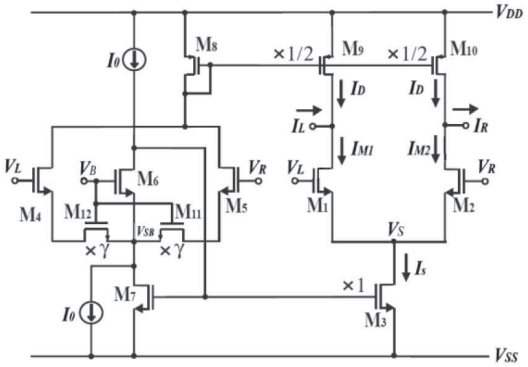


Fig.4 Proposed Transconductor

4. Proposed transconductor

From eq. (22) and Fig.3, it should be noticed that the transconductance deviation for low operating currents increases according as amplitude of the input voltage V_{in} increases. In order to alleviate the problem, the smaller tail current I_S at high amplitude of the input voltage is needed. Therefore, a new design of the square current source to realize such a tail current I_S is proposed.

Fig.4 shows the proposed transconductor, which is realized by introducing MOS resistors M11 and M12 into the transconductor shown in Fig.2 The MOS resistors are employed to control the tail current I_S supplied to the differential pair, which is different from the source degeneration operating. The gate nodes are connected to V_B. Because M11 and M12 operate in the triode region, the drain currents are expressed as

$$I_{M(11,12)} = 2\gamma V_N\left(-V_{SB} - V_T - \frac{V_{DS}}{2}\right)V_{DS}, \quad (23)$$

where γ is the aspect ratio of M11 and M12. V_{DS} is the drain-source voltage of M11 and M12. From (23), the equivalent resistance R_{eq} is expressed as

$$R_{eq} = \frac{1}{\frac{dI_{M(11,12)}}{dV_{DS}}} = \frac{1}{2\gamma K_N(-V_{SB}-V_T-V_{DS})}. \quad (24)$$

The drain currents of M4 and M5 are expressed as

$$I_{M4} = I_{D0}\exp\left(\frac{V_L - V_{SB} - R_{eq}I_{M4} - V_T}{nU_T}\right)$$
$$I_{M5} = I_{D0}\exp\left(\frac{V_R - V_{SB} - R_{eq}I_{M5} - V_T}{nU_T}\right). \quad (25)$$

From (12) and (25), the tail current I_S realized by the square current source is expressed as

$$I_S = \frac{nU_T}{R_{eq}}(W(B_1) - W(B_2)) \ , \tag{26}$$

where

$$B_1 = \frac{\exp\left(\frac{2\sqrt{I_0/K_N} - V_{in}}{2nU_T}\right) I_{D0}R_{eq}}{nU_T}$$

$$B_2 = \frac{\exp\left(\frac{2\sqrt{I_0/K_N} + V_{in}}{2nU_T}\right) I_{D0}R_{eq}}{nU_T} \ ,$$

and W(z) is the Lambert' s W function, which is defined as

$$z = W(z)\exp\big(W(z)\big) \ . \tag{27}$$

Substituting (26) into (18), the source voltage VS is rewritten as

$$V_S = \frac{V_{in}}{2} - V_T + nU_T \log\left[\frac{I_{D0}R_{eq}\left(1+\exp\left(\frac{-V_{in}}{nU_T}\right)\right)}{nU_T(W(B_1)-W(B_2))}\right] . \tag{28}$$

From (16) and (28), the drain currents of M1 and M2 are expressed as

$$I_{M1} = nU_T\left[\frac{W(B_1)+W(B_2)}{R_{eq}\left(1+\exp\left(\frac{-V_{in}}{2}\right)\right)}\right]$$

$$I_{M2} = nU_T\left[\frac{W(B_1)-W(B_2)}{R_{eq}\left(1+\exp\left(\frac{V_{in}}{2}\right)\right)}\right] \ . \tag{29}$$

From (29), the output current I_{out} is expressed as

$$I_{out} = \frac{nU_T}{R_{eq}}\tanh\left(\frac{V_{in}}{2nU_T}\right)(W(B_1) + W(B_2)). \tag{30}$$

The transconductance is expressed as

$$G_m = \frac{1}{2R_{eq}}\left(\frac{W(B_1)+W(B_2)}{\cosh\left(\frac{V_{in}}{2nU_T}\right)}\right) + \frac{1}{2R_{eq}}\left[\frac{\left(-W(B_1)+W(B_2)\right)\tanh\left(\frac{V_{in}}{2nU_T}\right)}{(1+W(B_1)(1+W(B_2))}\right] . \tag{31}$$

An equation for optimization of γ using maximally flat approximation method [7] is obtained as

$$\frac{d^2G_m}{dV_{in}{}^2}\Big|_{(V_{in}=0)} = 0 \ . \tag{32}$$

Solving (32), the optimum value of R_{eq} is given by

$$R_{eq} = \frac{nU_T}{7I_{D0}}\exp\left(\frac{nU_T - 7\sqrt{I_0/K_N}}{7nU_T}\right) \ . \tag{33}$$

From (24) and (33), the optimum value of γ is obtained as

$$\gamma = \frac{7I_{D0}\exp\left(\frac{7\sqrt{I_0/K_N} - nU_T}{7nU_T}\right)}{2nU_TK_N(-V_{DS}-V_S-V_T)} \ . \tag{34}$$

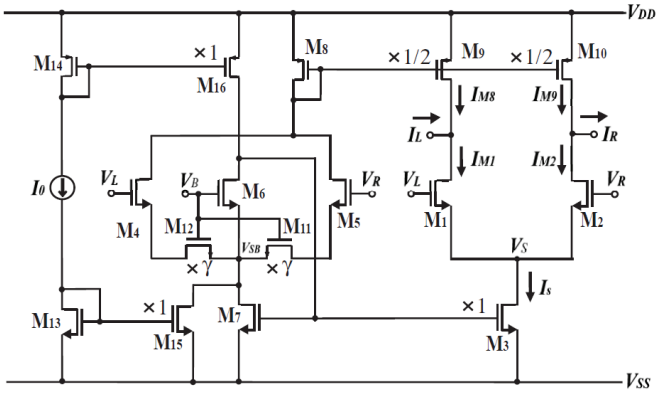


Fig.5 Circuit Configuration of Proposed Transconductor

Table 1 Principle Parameters of Used Model

K_M [$\mu A/V^2$]	V_T [V]	U_T [mV]	n	I_{D0} [μA]
121	0.41	26.0	1.47	4.62

5. Simulation

In order to confirm the validity of the proposed technique, simulation was carried out. The used program software is SIMetrix. In simulation, 0.18μm BSIM3 Model is used[8]. The principal parameters of used model are listed in Table 1. The supply voltage is ±0.9V. The circuit configuration of the proposed transconductor used in simulation is shown in Fig.5. The optimum aspect ratio of the MOS resistors obtained from (34) is γ = 19.08. In the simulation, γ is set to 19. The transconductance error G_{mer}[%] is defined as

$$G_{mer} = \left(\frac{G_{mmax} - G_{mmin}}{G_m(0)}\right) \times 100 \qquad (35)$$

where G_{mmax} and G_{mmin} are the maximum Gm and the minimum G_m in the input range, respectively. $G_m(0)$ is the G_m at V_{in} = 0 V. The input range is ± 1.0 V.

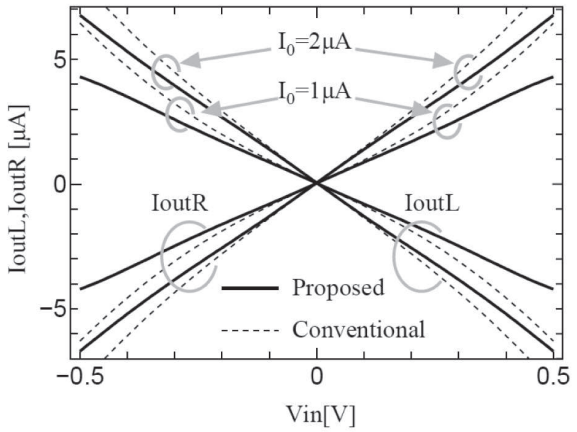


Fig.6 Transfer Characteristic

Table 2 Transconductance Error G_{mer}

G_{mer} for each of I_0	1μA [%]	3μA [%]	5μA [%]	9μA [%]
Proposed	9.226	5.802	7.493	5.755
Conventional	102.2	25.17	7.545	5.258

Fig.6 illustrates transfer characteristics of the proposed transconductor. It is seen from Fig.6 that the linearity deterioration for low operating currents is improved using the proposed technique. Fig.7 illustrates normalized transconductance characteristics (Gm/Gm(0)). The transconductance errors are listed in Table 2. From Fig.7 and Table 1, it should be noticed that the proposed transconductor has good linearity compared with that of the conventional transconductor. This means that the MOS resistors are effective for the low operating currents while they affect the transfer characteristics little for the high operating currents. Fig.8 illustrates normalized transconductance characteristics of the proposed transconductor for various γ. It is seen that element sensitivities of the MOS resistors are small. The total harmonic distortions (THDs) of the conventional transconductor and the proposed one are plotted in Fig.9 for I0 = 1μA. The sinusoidal input is 10kHz and the input signal amplitude is 0.1V – 0.5V. It should be noticed from Fig.9 that the THD of the proposed transconductor is improved.

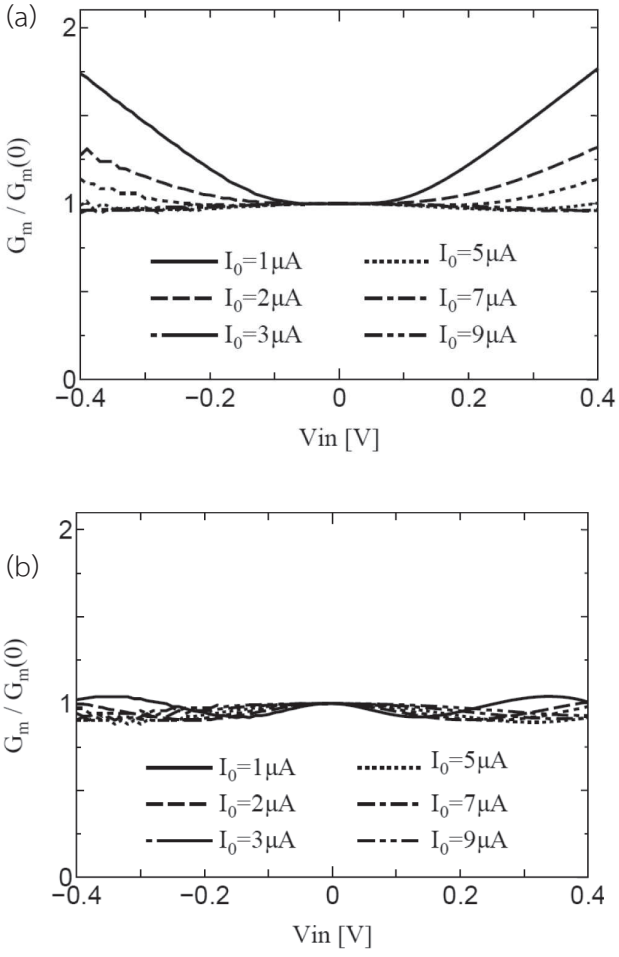


Fig.7 Normalized Transconductance Characteristics

(a) Conventional Transconductor

(b) Proposed Transconductor

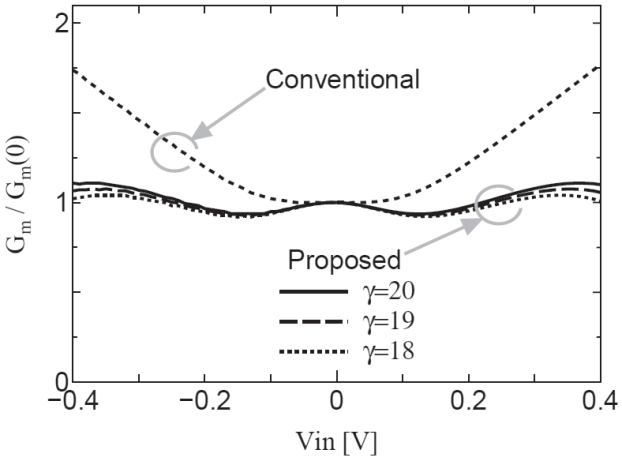


Fig.8 Normalized Gm characteristics for various γ

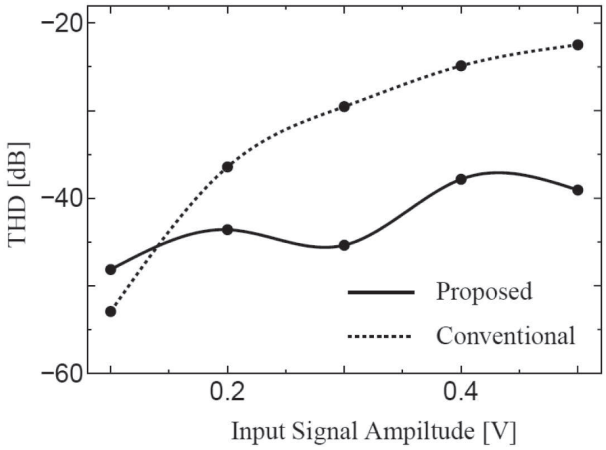


Fig.9 Total Harmonic Distortions (THDs)

6. Conclusion

In this paper, a new design of the adaptively biased linear MOS transconductor considering the influence of MOSFETs operating in weak inversion has been proposed. For low operating current, MOSFETs operate in weak inversion, and the voltage-current characteristic is not expressed as the square-law characteristic but is expressed as the exponential function. Thus, the factor makes linearity worse. In the proposed technique, the adaptive biasing circuit has newly designed for improvement of the linearity deterioration. Simulation results have shown that the proposed technique is effective for improvement of the linearity.

7. Acknowledgement

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8. References

(1) S.Susanta, 2005. Adaptively Biased Linear Transconductor, IEEE Transactions on Circuits and Systems, Vol.52, No.11, p.2369–2375.

(2) T. Pravit 2010. A New Adaptively Biased Linear MOS Transconductor Composed of a Square Current Source and a Differential Pair, The 23rd Workshop on Circuit and Systems, Ba1–2–2, p.73–78.

(3) A. Nedungadi, 1984. Design of linear CMOS transconductance elements. IEEE Transactions on Circuits and Systems, Oct. 1984, Vol. 31, No. 10, p. 891–894.

(4) A. M. Ismail, 2000. Novel CMOS Wide Linear Range Transconductance Amplifier, IEEE Transactions on Circuits and Systems, Aug. 2000, Vol. 47, No. 8 p. 1248–1253.

(5) Y. Cheng, M.C. Jeng, Z. Liu, J. Huang, M. Chan, K. Chen, P.K. Ko, C. Hu, 1997. A physical and scalable I-V model in BSIM3v3 for analog/digital circuit simulation, IEEE Transaction on Electron Devices, Vol.44, No. 2, p. 277–287.

(6) W. Liu, X. Jin, J. Chen, M.C. Jeng, Z. Liu, Y. Cheng, K. Chen, M. Chan, K. Hui, J. Huang, R. Tu, P.K. Ko, C. Hu, 1999. BSIM3v3.2.2 MOSFET Model User's Manual, University of California, Berkeley.

(7) H. Tanimoto, 1991. Realization of a 1-V Active Filter Using a Linearization Technique Employing Plurality of Emitter–Coupled Pairs, IEEE Journal of Solid-State Circuits, Jul. 1991, Vol. 26, p. 937–945.

(8) https://www.mosis.com/Thenical/Testdata/tsmc-018-prm.html.